

COMPAL CONFIDENTIAL

MODEL NAME : DAZ20 (SBMLK 12) / DAZ30 (SBMLK 13)

PCB NO : LA-F311P

BOM P/N : 431A8V31L0X (12_AR)
431A8V31L5X (13_AR)

Steamboat MLK 12"/13" AR

Kabylake-U U22 & Kabylake-R U42

2017-12-29

REV : 2.0 (A01)

@ : Nopop Component
EMI@ : EMI Component
@EMI@ : EMI Nopop Component
ESD@ : ESDComponent
@ESD@ : ESD Nopop Component
RF@ : RF Component
@RF@ : RF Nopop Component
CXDP@ : XDP Component
CONN@ : Connector Component
ESPI@ : ESPI interface Component
LPC@ : External ESPI Component (SHD)
U42@ : KBL-R U42 Component
U22@ : KBL-R U22 Component
SB12@ : For SB12 System ID
SB13@ : For SB13 System ID
DS3@ : Deep sleep Component
NDS3@ : Non Deep sleep Component

MB PCB

Part Number	Description
DAA000EJ010	PCB 263 LA-F311P REV0 MB AR 1

Layout Dell logo



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REV:A01
PWB: GD1PC

Power CKT : 0919
GPIO map : 0821

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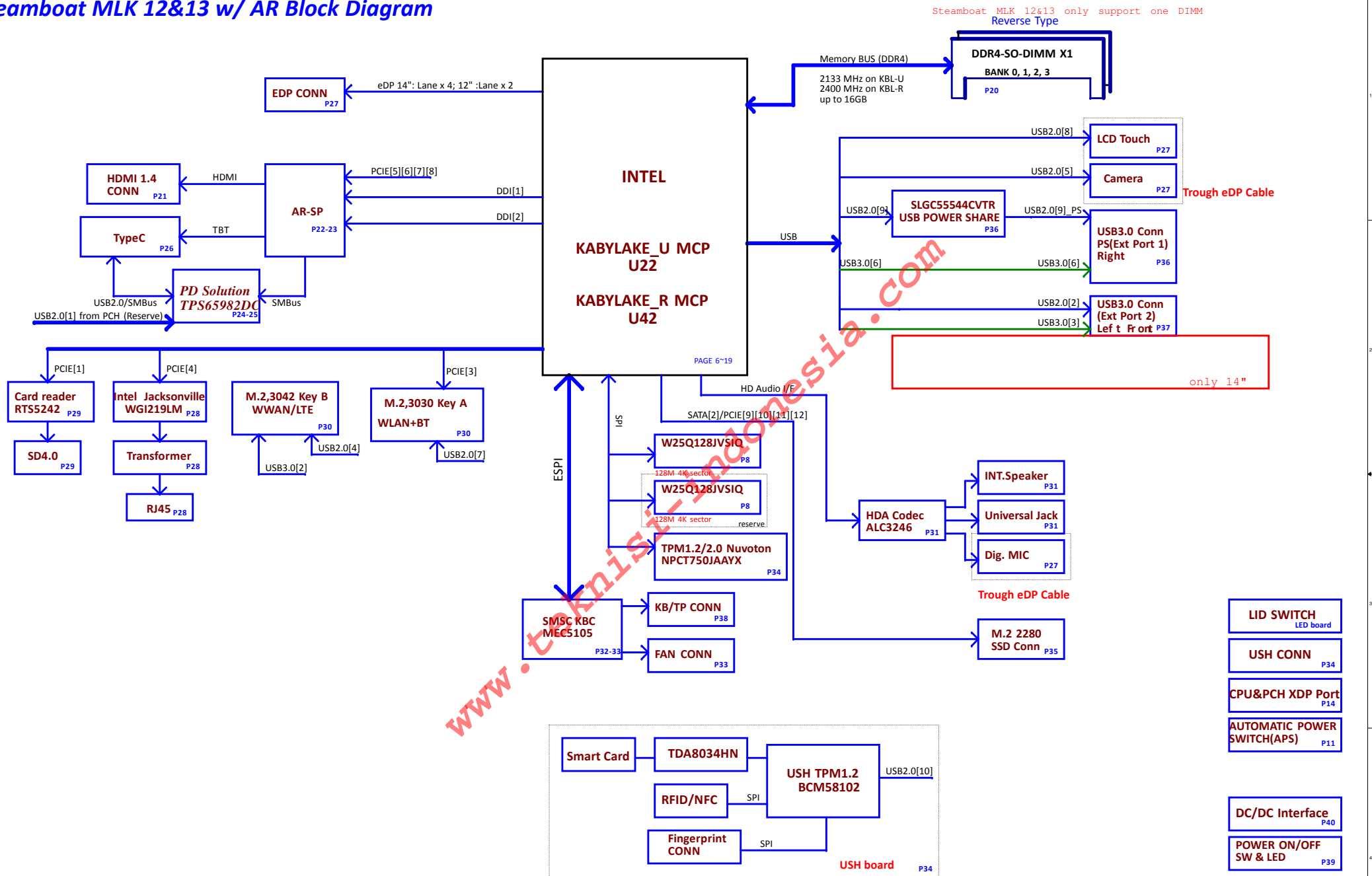


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Steamboat MLK 12&13 w/ AR Block Diagram



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Block diagram			
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POWER STATES

Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
State									
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	NP-155F	0.50
			Add Plating		
1	Top		Copper foil	0.5+plating	1.60
		3.7	Prepreg	1086 or 1086	2.95
2	GND/PWR		Copper foil	0.5oz	0.65
		3.9	Core	4mil	4.00
3	IN 1		Copper foil	0.5oz	0.65
		3.8	Prepreg	2113	3.35
4	GND/PWR		Copper foil	0.5oz	0.65
		4	Core	4mil	4.00
5	IN 2		Copper foil	0.5 oz	0.65
		4.2	Prepreg	2113	3.01
6	IN 3		Copper foil	0.5 oz	0.65
		3.7	Core	4mil	4.00
7	GND/PWR		Copper foil	0.5oz	0.65
		3.8	Prepreg	2113	3.35
8	IN 4		Copper foil	0.5oz	0.65
		3.9	Core	4mil	4.00
9	GND/PWR		Copper foil	0.5oz	0.65
		3.7	Prepreg	1086 or 1086	2.95
10	Bottom		Copper foil	0.5+plating	1.60
			Add Plating		
			SolderMask		0.50
	Overall Thickness (1.05mm ± 10%)		39.37		41.01000

1.041654

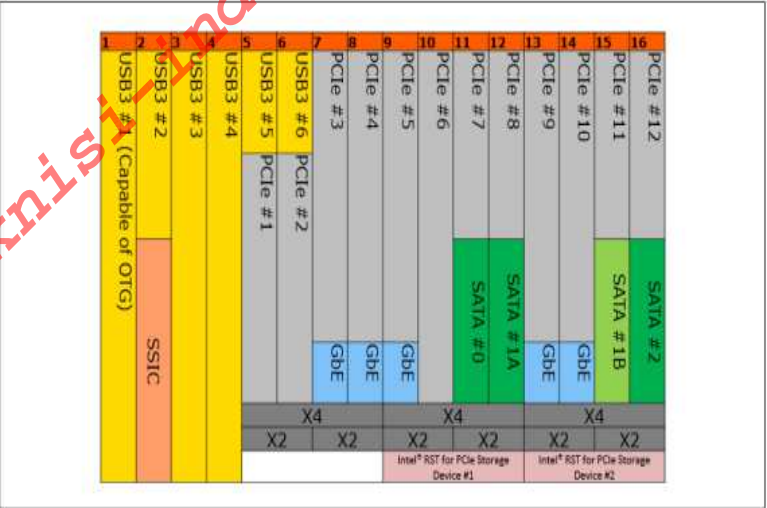
AR config

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				N/A
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Left Front
USB3.0-4				JUSB3-->Left Rear (SB14 only)
USB3.0-5		PCIE-1		Card Reader (PCIE)
USB3.0-6		PCIE-2		JUSB1-->Right
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		LOM
		PCIE-5		Alpine Ridge - SP
		PCIE-6		
		PCIE-7	SATA-0	
		PCIE-8	SATA-1	
		PCIE-9		M.2 2280 SSD (PCIex4 or SATA)
		PCIE-10		
		PCIE-11	SATA-1*	
		PCIE-12	SATA-2	

12" max support JUSB3

USB PORT#	DESTINATION
1	Reserve for Type C
2	JUSB2-->Left Front
3	JUSB3-->Left Rear (SB14 only)
4	M2 3042(WWAN)
5	Camera
6	NA
7	M.2 3030(BT)
8	Touch Screen
9	JUSB1-->Right
10	USH

High Speed I/O (HSIO) Lane Multiplexing in KBL U

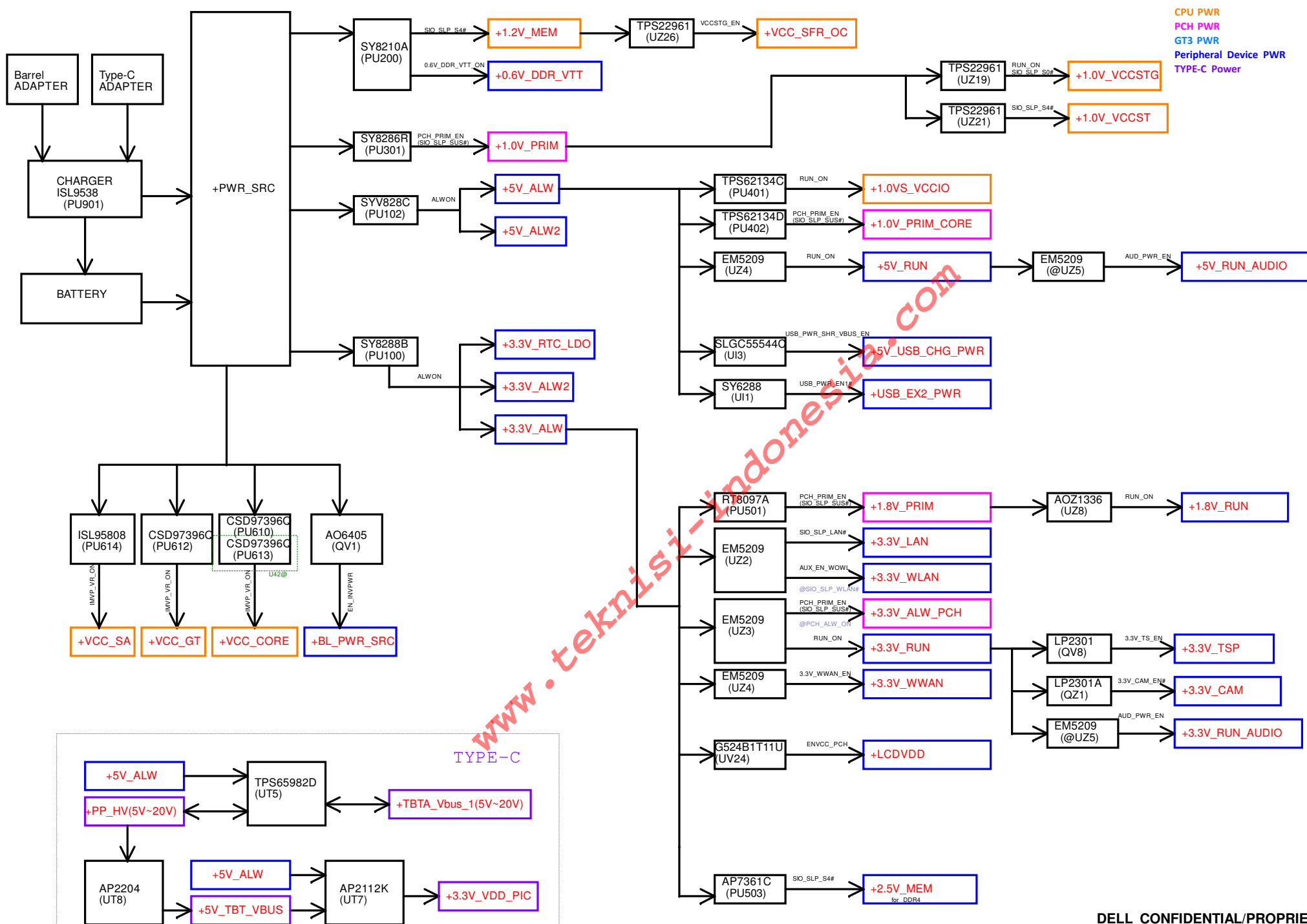


AR use 1086PP (10L)
Non AR use 1080PP (8L)

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Port assignment	
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CPU PWR
PCH PWR
GT3 PWR
Peripheral Device PWR
TYPE-C Power

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DDR4, Ballout for side by side(Interleave)

<20> DDR_A_DQS#[0..7] <<>>

<20> DDR_A_D[0..63] <<>>

<20> DDR_A_DQS[0..7] <<>>

<20> DDR_A_MA[0..16] <<>>

UC1B CPU@	KBL-R U4+2	Rev. 0.1
DDR_A_D0 AL71	DDR0_DQ[0]	DDR0_CKN[0]
DDR_A_D1 AL68	DDR0_DQ[1]	DDR0_CKN[1]
DDR_A_D2 AN68	DDR0_DQ[2]	DDR0_CKN[2]
DDR_A_D3 AN69	DDR0_DQ[3]	DDR0_CKN[3]
DDR_A_D4 AL70	DDR0_DQ[4]	DDR0_CKN[4]
DDR_A_D5 AL69	DDR0_DQ[5]	DDR0_CKN[5]
DDR_A_D6 AN70	DDR0_DQ[6]	DDR0_CKN[6]
DDR_A_D7 AN71	DDR0_DQ[7]	DDR0_CKN[7]
DDR_A_D8 AR70	DDR0_DQ[8]	DDR0_CKN[8]
DDR_A_D9 AH68	DDR0_DQ[9]	DDR0_CKN[9]
DDR_A_D10 AU71	DDR0_DQ[10]	DDR0_CKN[10]
DDR_A_D11 AU68	DDR0_DQ[11]	DDR0_CKN[11]
DDR_A_D12 AR71	DDR0_DQ[12]	DDR0_CKN[12]
DDR_A_D13 AR69	DDR0_DQ[13]	DDR0_CKN[13]
DDR_A_D14 AU70	DDR0_DQ[14]	DDR0_CKN[14]
DDR_A_D15 AU69	DDR0_DQ[15]	DDR0_CKN[15]

Interleave / Non-Interleave	DDR0 / LPDDR3 / DDR4	Rev. 0.1
DDR_A_D16 BB65	DDR0_MA[5]DDR0_CAA[0]DDR0_MA[5]	BA51 DDR_A_MA5
DDR_A_D17 AW65	DDR0_MA[9]DDR0_CAA[1]DDR0_MA[9]	BB54 DDR_A_MA9
DDR_A_D18 AW63	DDR0_MA[6]DDR0_CAA[2]DDR0_MA[6]	BA52 DDR_A_MA6
DDR_A_D19 AV63	DDR0_MA[8]DDR0_CAA[3]DDR0_MA[8]	AY62 DDR_A_MA8
DDR_A_D20 BA68	DDR0_MA[7]DDR0_CAA[4]DDR0_MA[7]	AW52 DDR_A_MA7
DDR_A_D21 AV65	DDR0_MA[2]DDR0_CAA[5]DDR0_MA[2]	AY65 DDR_A_MA2
DDR_A_D22 BA63	DDR0_MA[11]DDR0_CAA[6]DDR0_MA[11]	AW54 DDR_A_MA11
DDR_A_D23 BB63	DDR0_MA[14]DDR0_CAA[7]DDR0_MA[14]	BA55 DDR_A_MA14
DDR_A_D24 BA61	DDR0_MA[13]DDR0_CAB[0]DDR0_MA[13]	AY64 DDR_A_MA13
DDR_A_D25 AW61	DDR0_MA[10]DDR0_CAB[1]DDR0_MA[10]	AJ46 DDR_A_MA10
DDR_A_D26 BB59	DDR0_MA[15]DDR0_CAB[2]DDR0_MA[15]	AJ48 DDR_A_MA15
DDR_A_D27 AW59	DDR0_MA[6]DDR0_CAB[3]DDR0_MA[6]	AT46 DDR_A_MA6
DDR_A_D28 BB61	DDR0_MA[8]DDR0_CAB[4]DDR0_MA[8]	AJ50 DDR_A_MA8
DDR_A_D29 AV61	DDR0_MA[2]DDR0_CAB[5]DDR0_MA[2]	AY51 DDR_A_MA2
DDR_A_D30 BA59	DDR0_MA[11]DDR0_CAB[6]DDR0_MA[11]	AT48 DDR_A_MA11
DDR_A_D31 AY59	DDR0_MA[14]DDR0_CAB[7]DDR0_MA[14]	AT50 DDR_A_MA14
DDR_A_D32 AY39	DDR0_MA[13]DDR0_CAB[0]DDR0_MA[13]	BB50 DDR_A_MA13
DDR_A_D33 AW39	DDR0_MA[10]DDR0_CAB[1]DDR0_MA[10]	AY50 DDR_A_MA10
DDR_A_D34 AY37	DDR0_MA[15]DDR0_CAB[2]DDR0_MA[15]	BA50 DDR_A_MA15
DDR_A_D35 AW37	DDR0_MA[6]DDR0_CAB[3]DDR0_MA[6]	BB52 DDR_A_MA6
DDR_A_D36 BB39	DDR0_MA[8]DDR0_CAB[4]DDR0_MA[8]	AJ70 DDR_A_MA8
DDR_A_D37 BA39	DDR0_MA[2]DDR0_CAB[5]DDR0_MA[2]	AM69 DDR_A_MA2
DDR_A_D38 BA37	DDR0_MA[11]DDR0_CAB[6]DDR0_MA[11]	AT69 DDR_A_MA11
DDR_A_D39 BB37	DDR0_MA[14]DDR0_CAB[7]DDR0_MA[14]	AT70 DDR_A_MA14
DDR_A_D40 AY35	DDR0_MA[13]DDR0_CAB[0]DDR0_MA[13]	
DDR_A_D41 AY35	DDR0_MA[10]DDR0_CAB[1]DDR0_MA[10]	
DDR_A_D42 AY33	DDR0_MA[15]DDR0_CAB[2]DDR0_MA[15]	
DDR_A_D43 AW33	DDR0_MA[6]DDR0_CAB[3]DDR0_MA[6]	
DDR_A_D44 BB35	DDR0_MA[8]DDR0_CAB[4]DDR0_MA[8]	
DDR_A_D45 BA35	DDR0_MA[2]DDR0_CAB[5]DDR0_MA[2]	
DDR_A_D46 BA33	DDR0_MA[11]DDR0_CAB[6]DDR0_MA[11]	
DDR_A_D47 BB33	DDR0_MA[14]DDR0_CAB[7]DDR0_MA[14]	
DDR_A_D48 AY31	DDR0_MA[13]DDR0_CAB[0]DDR0_MA[13]	
DDR_A_D49 AW31	DDR0_MA[10]DDR0_CAB[1]DDR0_MA[10]	
DDR_A_D50 AY29	DDR0_MA[15]DDR0_CAB[2]DDR0_MA[15]	
DDR_A_D51 AW29	DDR0_MA[6]DDR0_CAB[3]DDR0_MA[6]	
DDR_A_D52 BB31	DDR0_MA[8]DDR0_CAB[4]DDR0_MA[8]	
DDR_A_D53 BA31	DDR0_MA[2]DDR0_CAB[5]DDR0_MA[2]	
DDR_A_D54 BA29	DDR0_MA[11]DDR0_CAB[6]DDR0_MA[11]	
DDR_A_D55 BB29	DDR0_MA[14]DDR0_CAB[7]DDR0_MA[14]	
DDR_A_D56 AY27	DDR0_MA[13]DDR0_CAB[0]DDR0_MA[13]	
DDR_A_D57 AW27	DDR0_MA[10]DDR0_CAB[1]DDR0_MA[10]	
DDR_A_D58 AY25	DDR0_MA[15]DDR0_CAB[2]DDR0_MA[15]	
DDR_A_D59 AW25	DDR0_MA[6]DDR0_CAB[3]DDR0_MA[6]	
DDR_A_D60 BB27	DDR0_MA[8]DDR0_CAB[4]DDR0_MA[8]	
DDR_A_D61 BA27	DDR0_MA[2]DDR0_CAB[5]DDR0_MA[2]	
DDR_A_D62 BA25	DDR0_MA[11]DDR0_CAB[6]DDR0_MA[11]	
DDR_A_D63 BB25	DDR0_MA[14]DDR0_CAB[7]DDR0_MA[14]	

DDR0_PAR,DDR0_ALERT# for DDR4

DDR_ALERT#

DDR_PAR

DDR_VREF_CA

DDR_VREF_DO

DDR_VREF_DQ

DDR_VTT_CTRL

UC1C CPU@	KBL-R U4+2	Rev. 0.1
Interleave / Non-Interleave	DDR1 / LPDDR3 / DDR4	Rev. 0.1
AF65	DDR1_DQ[0]DDR0_DQ[16]	AN45
AF64	DDR1_DQ[1]DDR0_DQ[17]	AN46
AK65	DDR1_DQ[2]DDR0_DQ[18]	AN47
AK64	DDR1_DQ[3]DDR0_DQ[19]	AN48
AF66	DDR1_DQ[4]DDR0_DQ[20]	AN56
AF67	DDR1_DQ[5]DDR0_DQ[21]	AP55
AK66	DDR1_DQ[6]DDR0_DQ[22]	AN57
AF70	DDR1_DQ[7]DDR0_DQ[23]	AP54
AF68	DDR1_DQ[8]DDR0_DQ[24]	DDR1_CKE[3]
AH71	DDR1_DQ[9]DDR0_DQ[25]	BB42
AH68	DDR1_DQ[10]DDR0_DQ[26]	DDR1_CS#0
AF71	DDR1_DQ[11]DDR0_DQ[27]	DDR1_CS#1
AF69	DDR1_DQ[12]DDR0_DQ[28]	DDR1_ODT[0]
DD1	DDR1_DQ[13]DDR0_DQ[29]	DDR1_ODT[1]
AH70	DDR1_DQ[14]DDR0_DQ[30]	
AH69	DDR1_DQ[15]DDR0_DQ[31]	
AT66	DDR1_DQ[16]DDR0_DQ[32]	
AU68	DDR1_DQ[17]DDR0_DQ[33]	
AP65	DDR1_DQ[18]DDR0_DQ[34]	
AN65	DDR1_DQ[19]DDR0_DQ[35]	
AN66	DDR1_DQ[20]DDR0_DQ[36]	
AP66	DDR1_DQ[21]DDR0_DQ[37]	
AT65	DDR1_DQ[22]DDR0_DQ[38]	
AU65	DDR1_DQ[23]DDR0_DQ[39]	
AT61	DDR1_DQ[24]DDR0_DQ[40]	
AU61	DDR1_DQ[25]DDR0_DQ[41]	
AP60	DDR1_DQ[26]DDR0_DQ[42]	
AN60	DDR1_DQ[27]DDR0_DQ[43]	
AU61	DDR1_DQ[28]DDR0_DQ[44]	
AP61	DDR1_DQ[29]DDR0_DQ[45]	
AT60	DDR1_DQ[30]DDR0_DQ[46]	
AU60	DDR1_DQ[31]DDR0_DQ[47]	
AT40	DDR1_DQ[32]DDR1_DQ[16]	
AT37	DDR1_DQ[33]DDR1_DQ[17]	
AU37	DDR1_DQ[34]DDR1_DQ[18]	
AR40	DDR1_DQ[35]DDR1_DQ[19]	
AP40	DDR1_DQ[36]DDR1_DQ[20]	
AP37	DDR1_DQ[37]DDR1_DQ[21]	
AR37	DDR1_DQ[38]DDR1_DQ[22]	
AT33	DDR1_DQ[39]DDR1_DQ[23]	
AJ33	DDR1_DQ[40]DDR1_DQ[24]	
AJ30	DDR1_DQ[41]DDR1_DQ[25]	
AT30	DDR1_DQ[42]DDR1_DQ[26]	
AR33	DDR1_DQ[43]DDR1_DQ[27]	
AP33	DDR1_DQ[44]DDR1_DQ[28]	
AR30	DDR1_DQ[45]DDR1_DQ[29]	
AP30	DDR1_DQ[46]DDR1_DQ[30]	
AT30	DDR1_DQ[47]DDR1_DQ[31]	
AU27	DDR1_DQ[48]	
AT27	DDR1_DQ[49]	
AT25	DDR1_DQ[50]	
AJ25	DDR1_DQ[51]	
AP27	DDR1_DQ[52]	
AN25	DDR1_DQ[53]	
AP25	DDR1_DQ[54]	
AJ22	DDR1_DQ[55]	
AN22	DDR1_DQ[56]	
AT21	DDR1_DQ[57]	
AN22	DDR1_DQ[58]	
AP22	DDR1_DQ[59]	
AT21	DDR1_DQ[60]	
AN21	DDR1_DQ[61]	
AN21	DDR1_DQ[62]	
AN21	DDR1_DQ[63]	

DDR4 COMPENSATION SIGNALS

SM_RCOMP0 RC5 1 2 121 0402 1%

SM_RCOMP1 RC6 1 2 80.6 0402 1%

SM_RCOMP2 RC7 1 2 100 0402 1%

CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length=500 mil

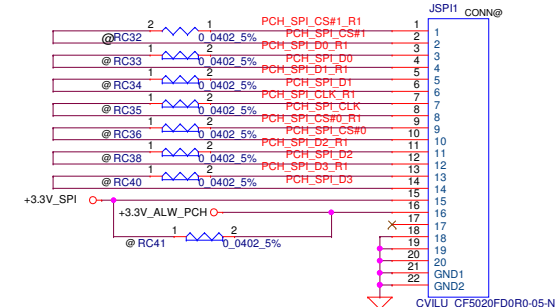
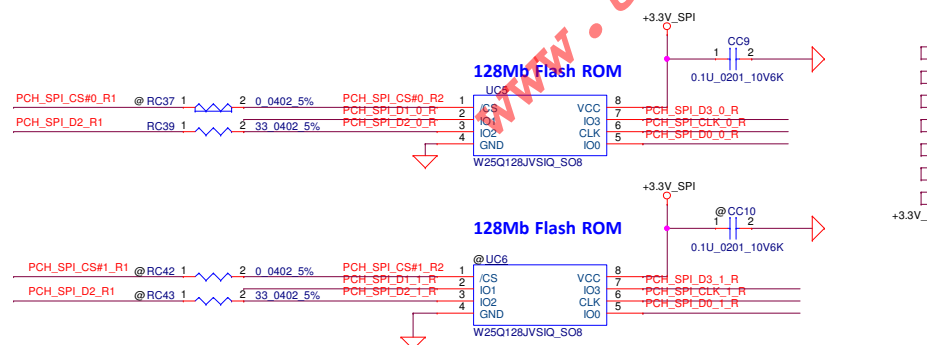
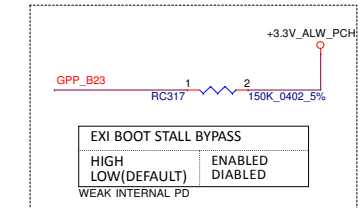
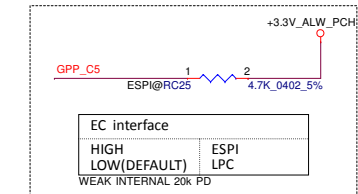
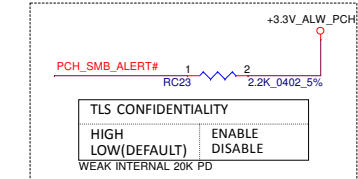
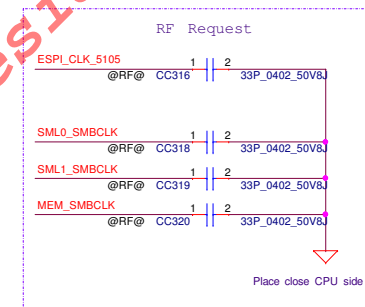
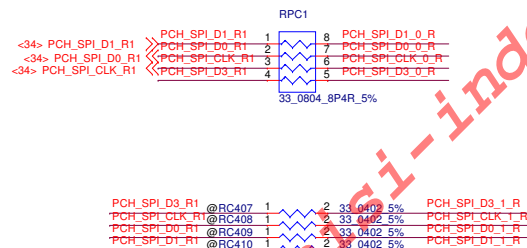
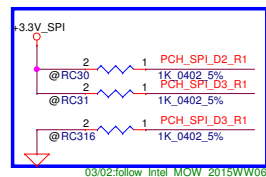
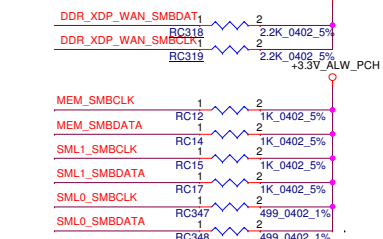
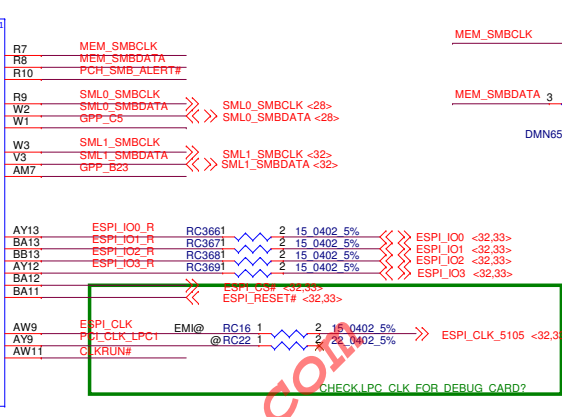
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CPU (2/14)		
Title	Document Number	Rev
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Date: Wednesday, December 20, 2017	Sheet 7 of 58	

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Rev	3.0
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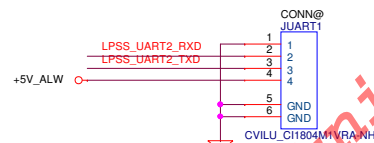
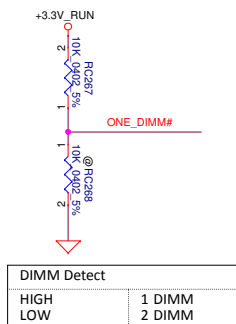
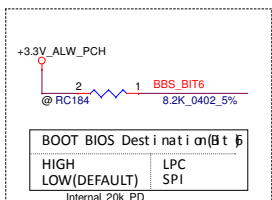
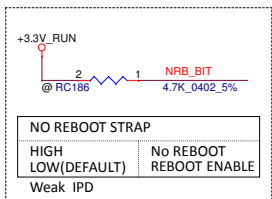
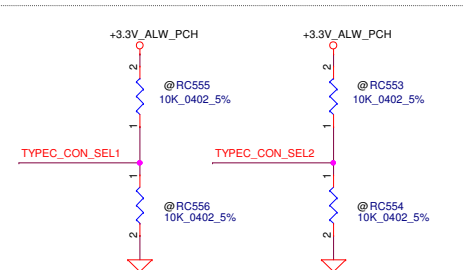


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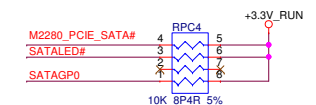
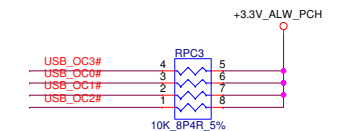
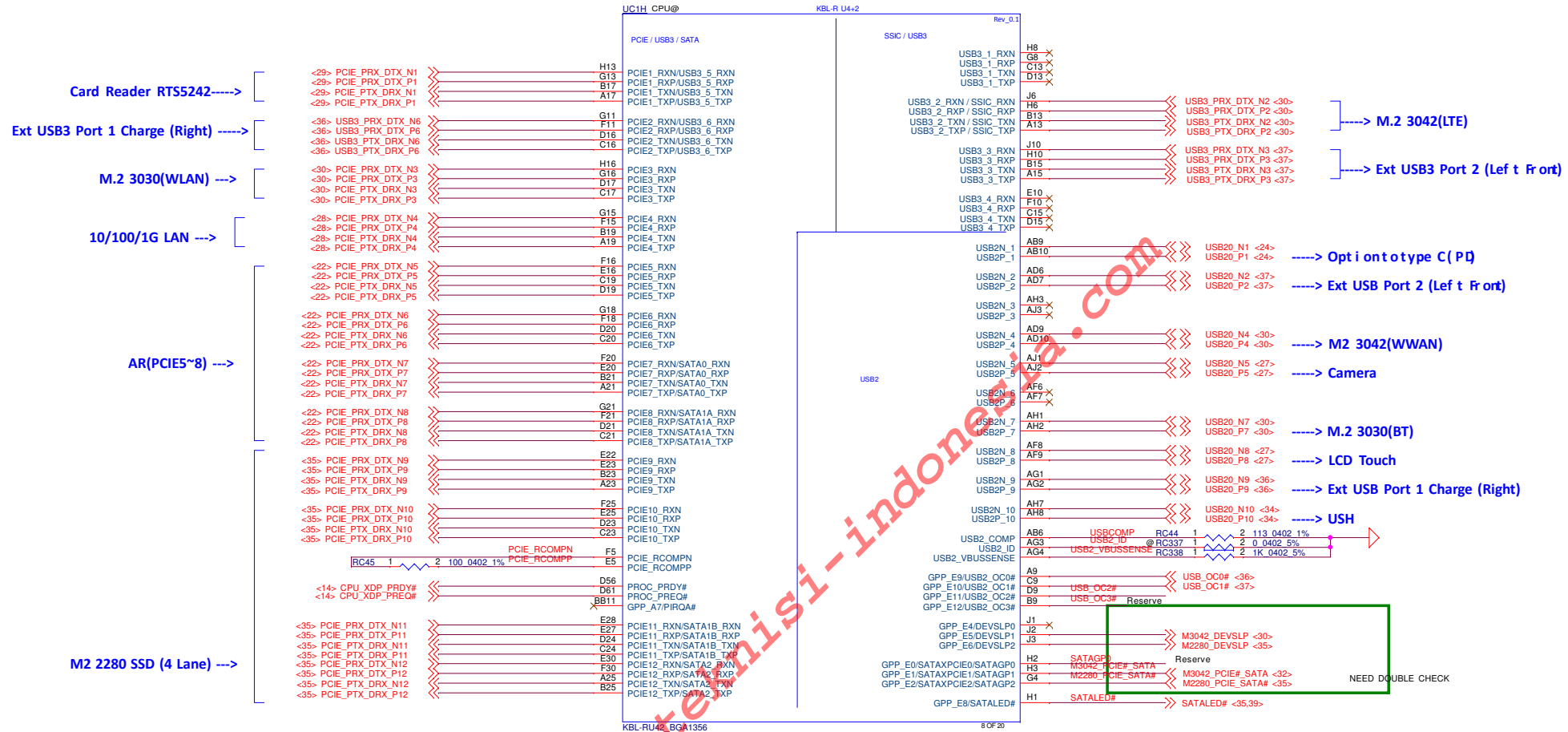
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Vendor	JAE	FOXCON	TBD	TBD
TYPEC_CON_SEL1	LOW	LOW	HIGH	HIGH
TYPEC_CON_SEL2	LOW	HIGH	LOW	HIGH



DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave

AR_DET#	
HIGH	NON AR
LOW	AR



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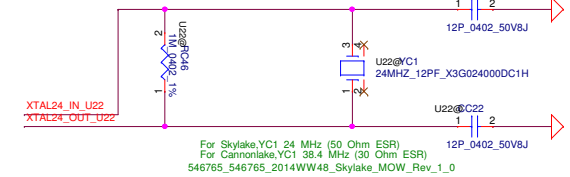


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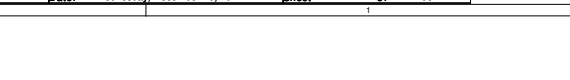
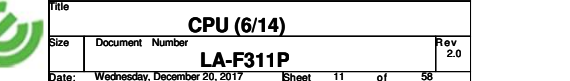
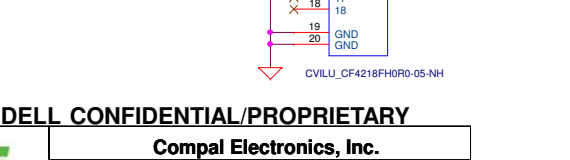
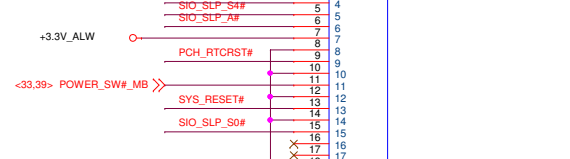
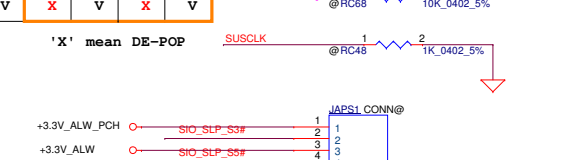
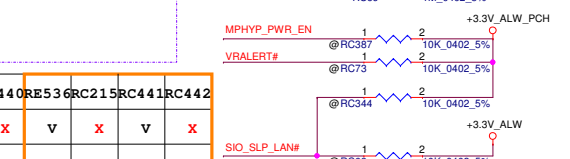
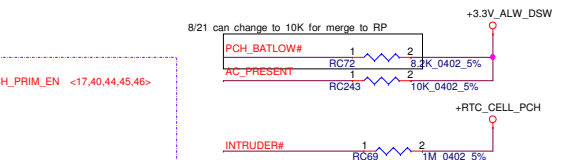
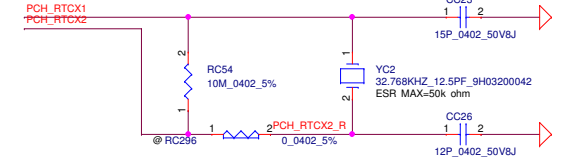
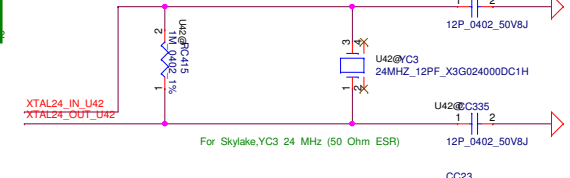
CPU (5/14)			Rev
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For KBL-R U22



For KBL-R U42



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CPU (6/14)

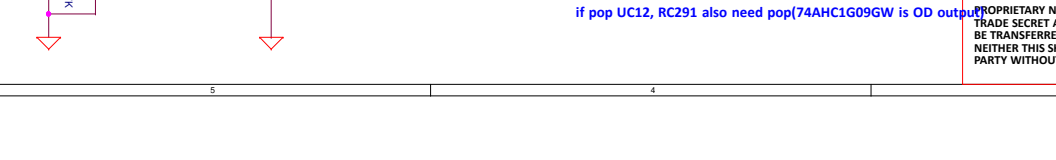
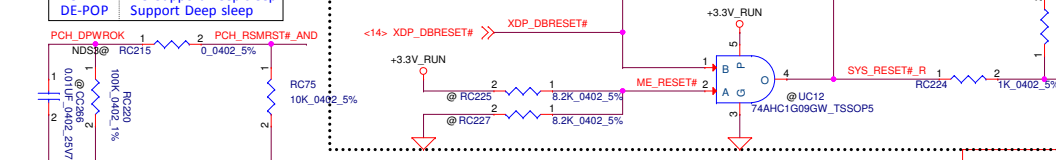
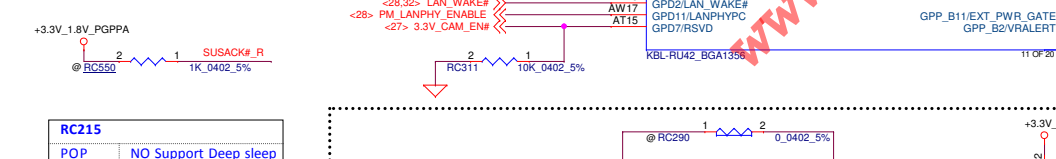
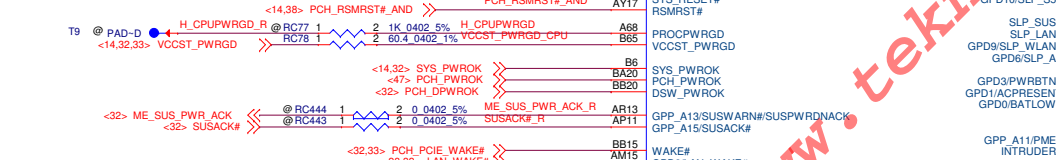
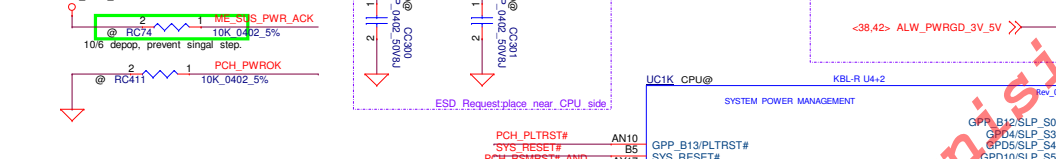
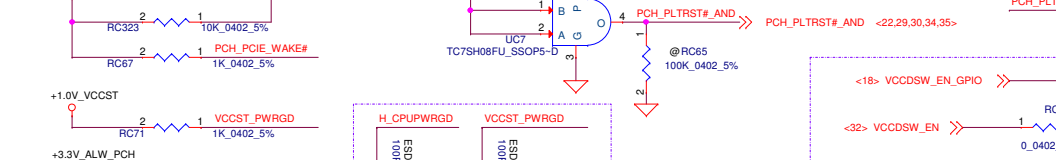
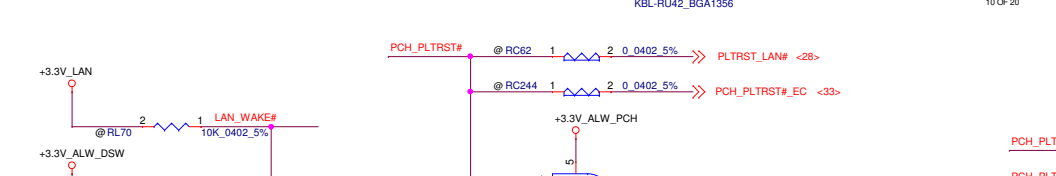
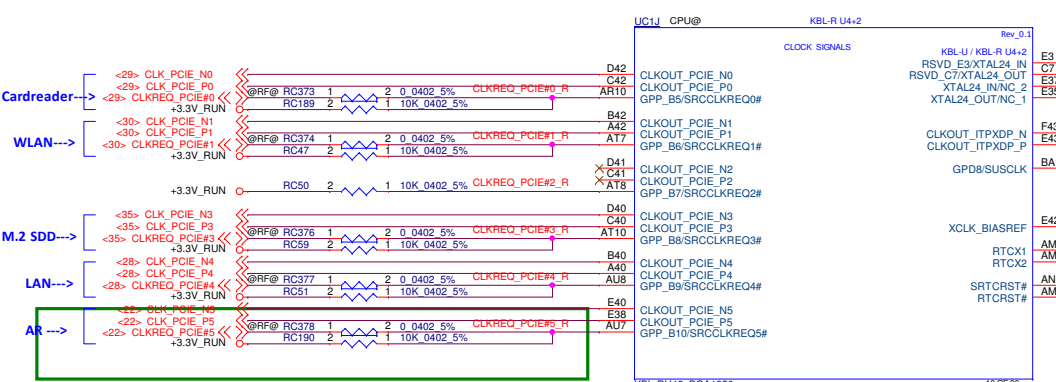
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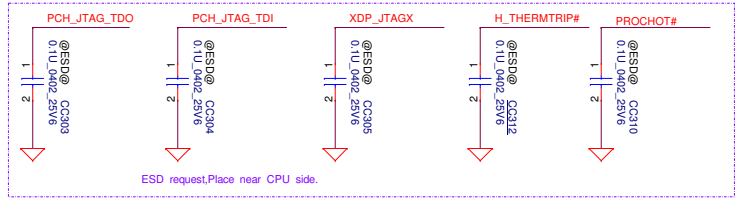
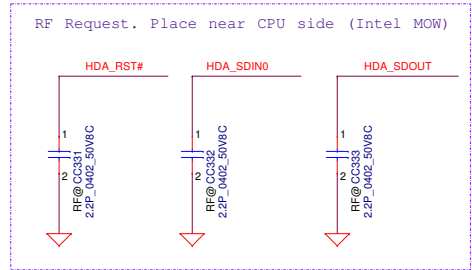
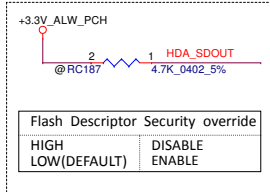
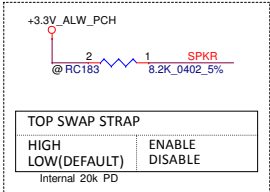
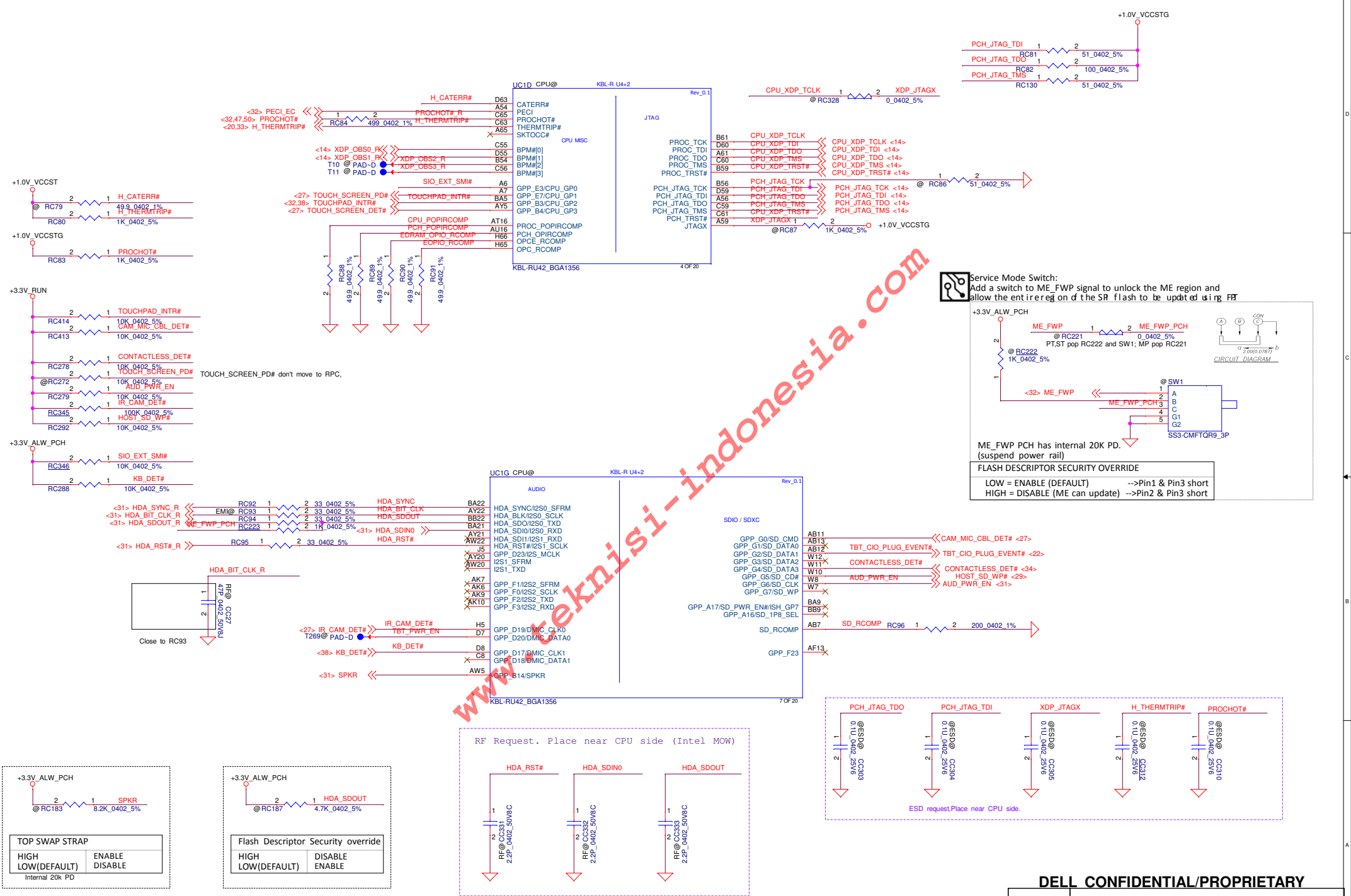
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if pop UC12, RC291 also need pop(74AHC1G09GW is OD output





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CPU (7/14)

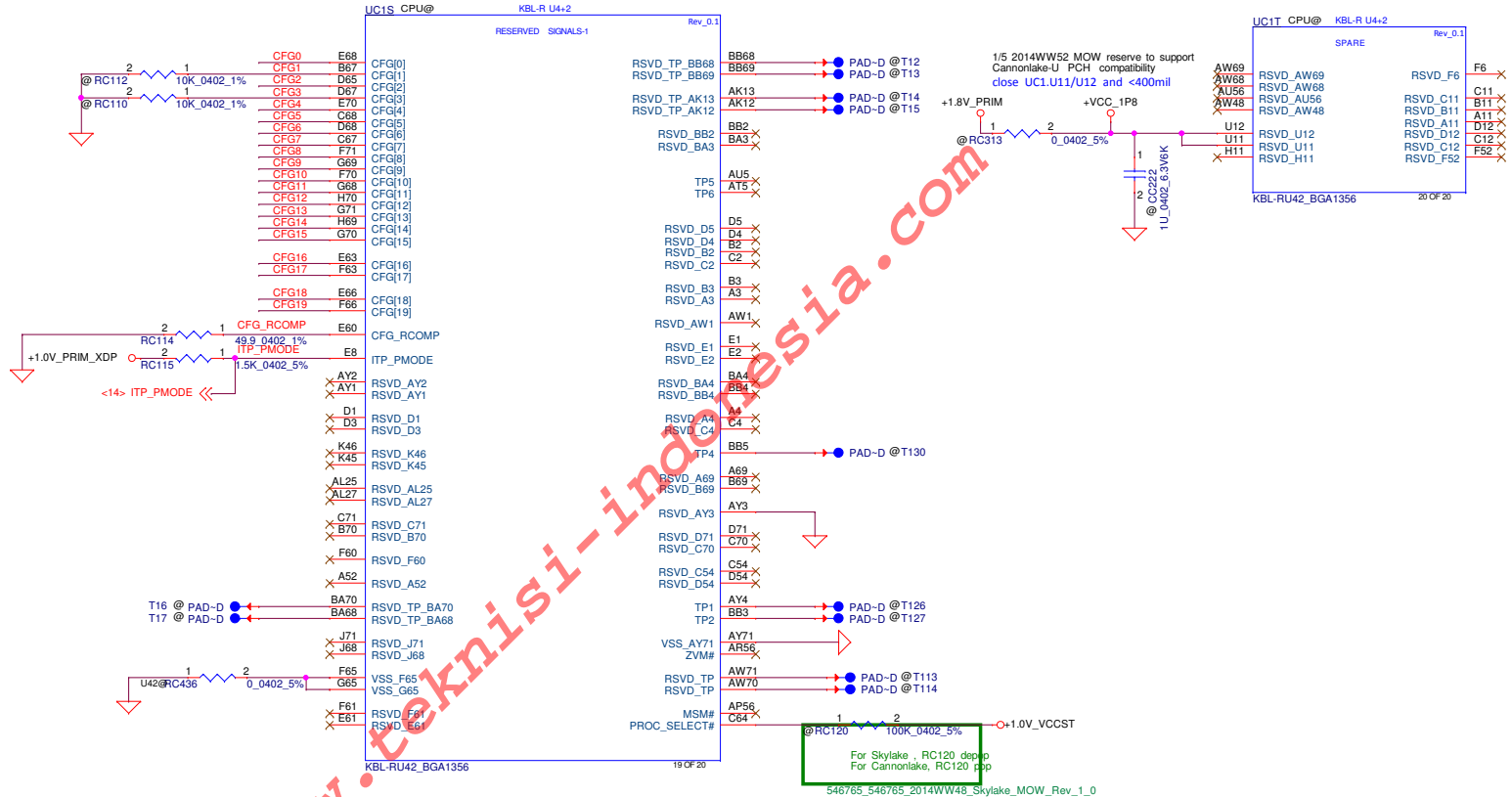
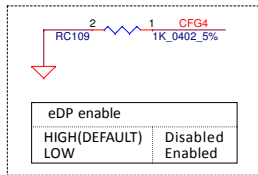
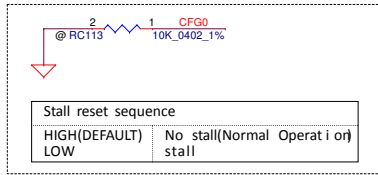
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<14> CFG0[0..19] <<

CFG2[5][6][7] for SKYLAKE-H CPU CFG strap pin



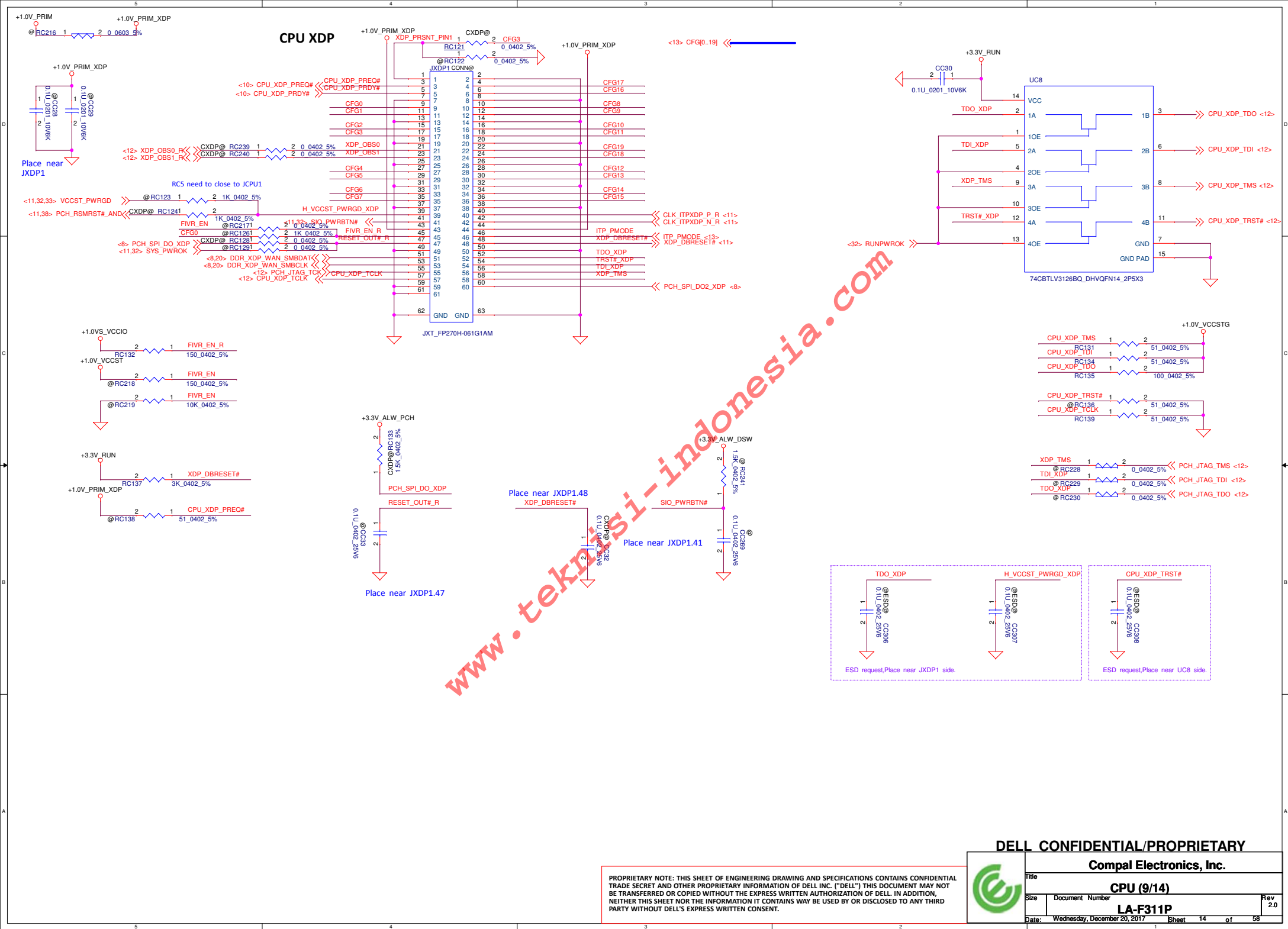
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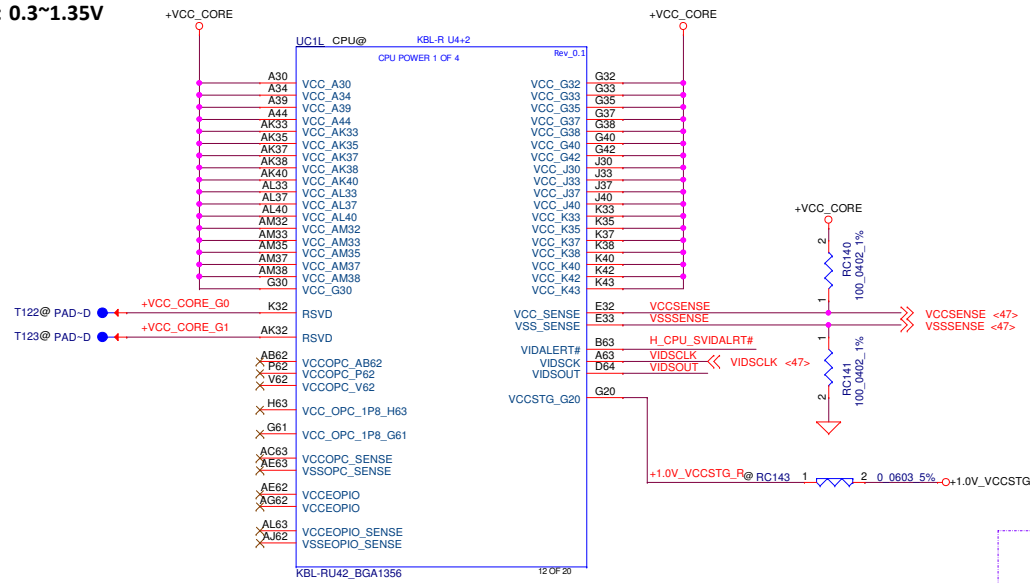


Title		
CPU (8/14)		
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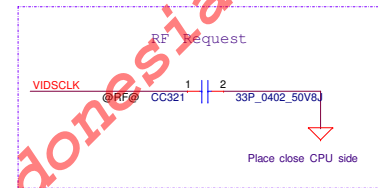


+VCC_CORE: 0.3~1.35V

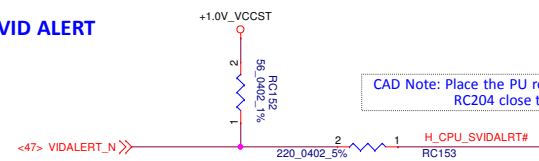


PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

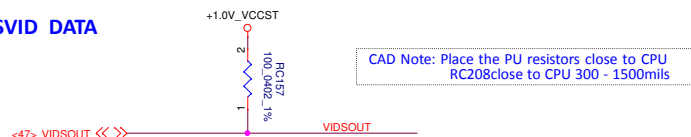
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source



SVID ALERT



SVID DATA



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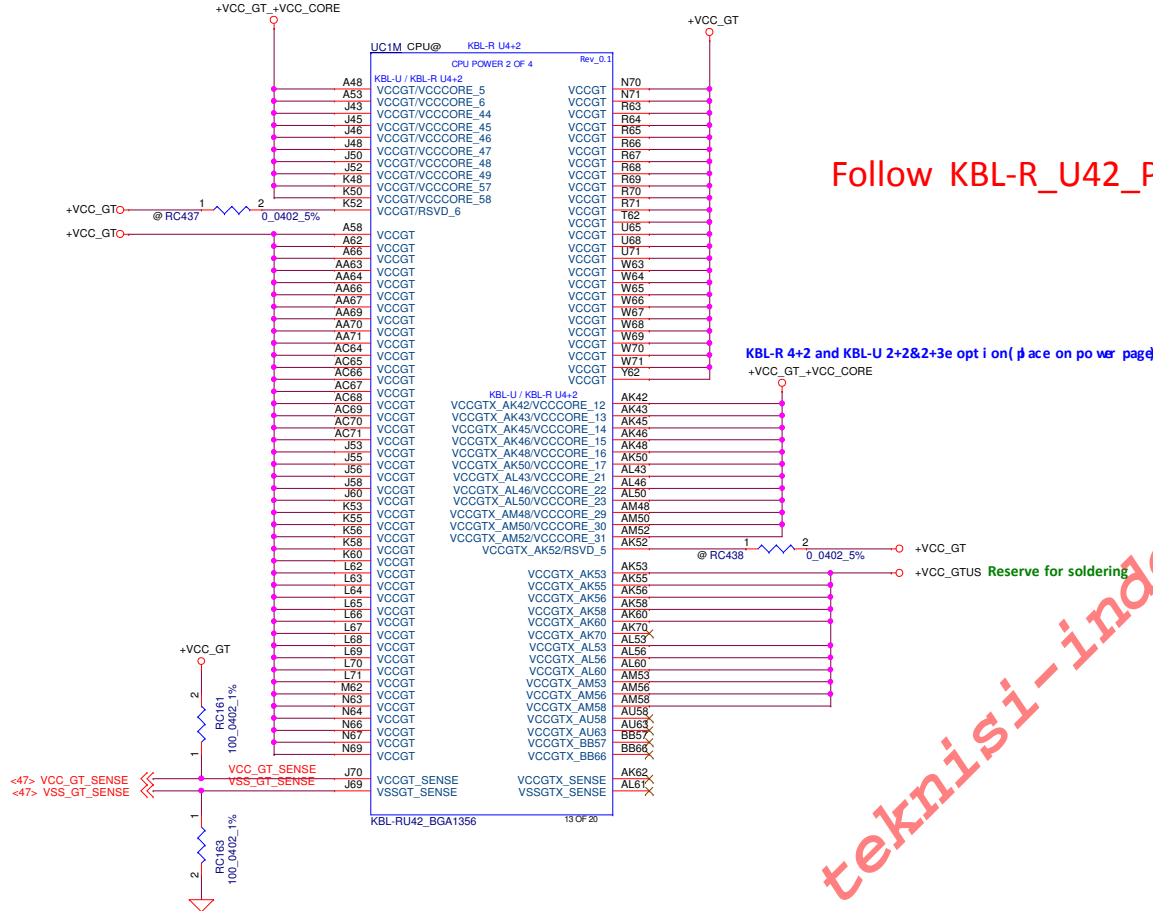
CPU (10/14)

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+VCCGT: 0.3~1.35V
+VCCGTx : 0.3~1.35V

KBL-R 4+2 and KBL-U 2+2&2+3e opt i on(p ace on po wer page)



Follow KBL-R_U42_Processor_Line_BGA1356_Ballout_Rev1p0

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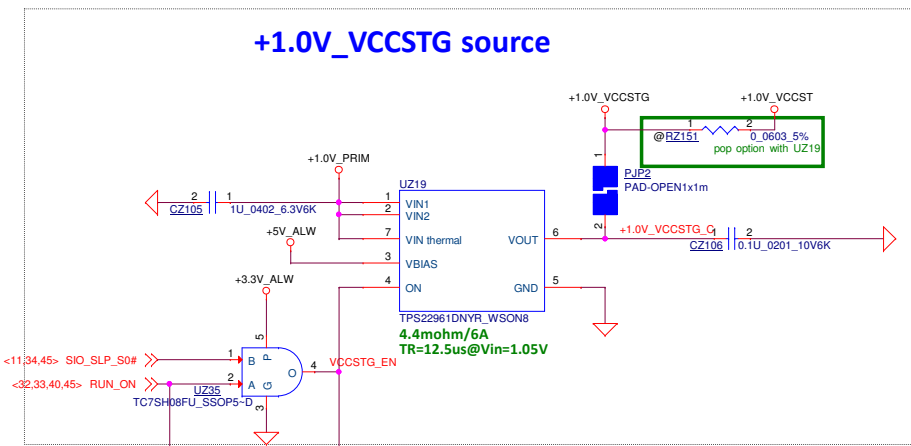
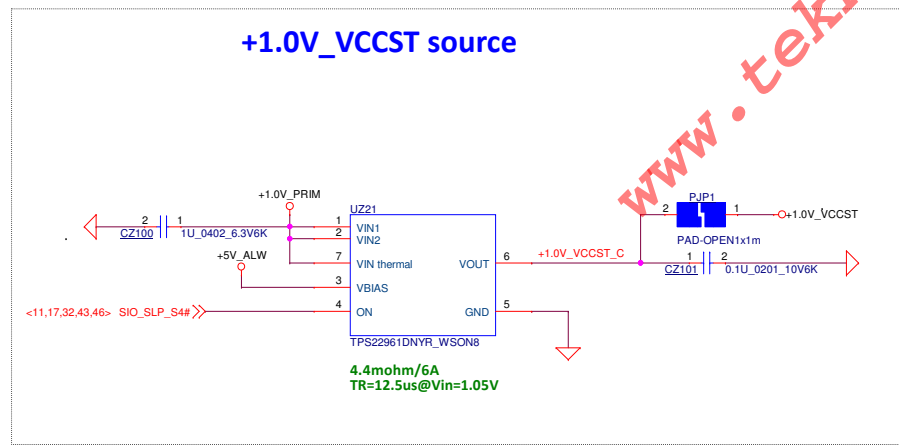
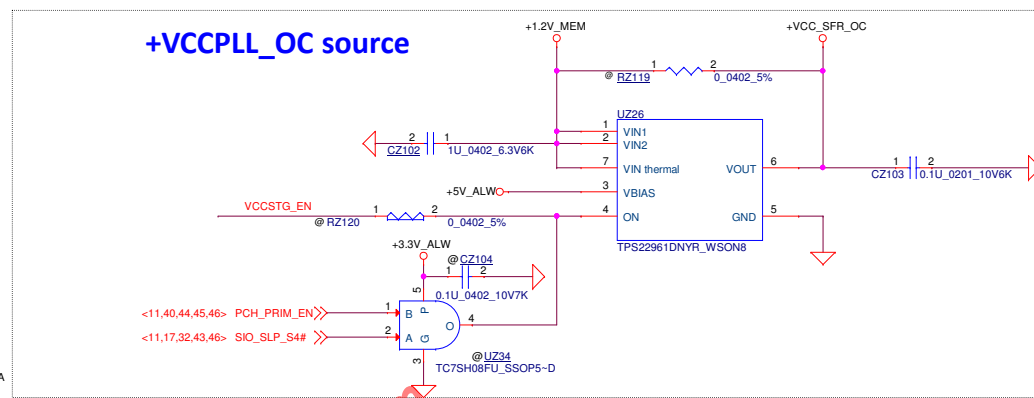
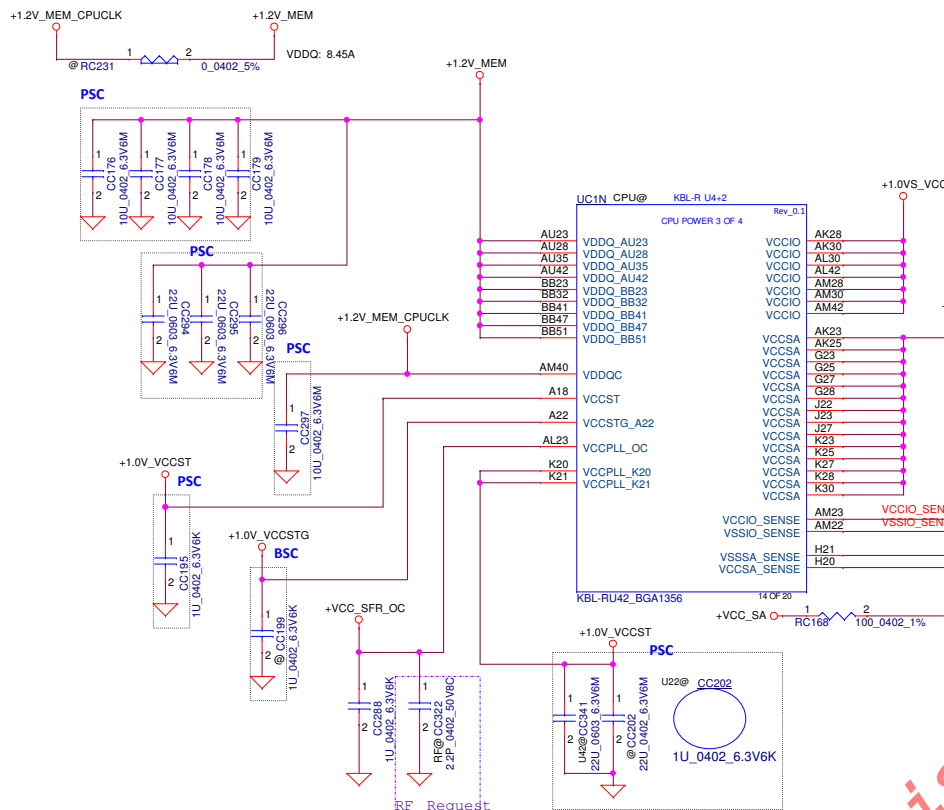
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	S0	S0Ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW

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CPU (12/14)

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Title

Size

Document Number

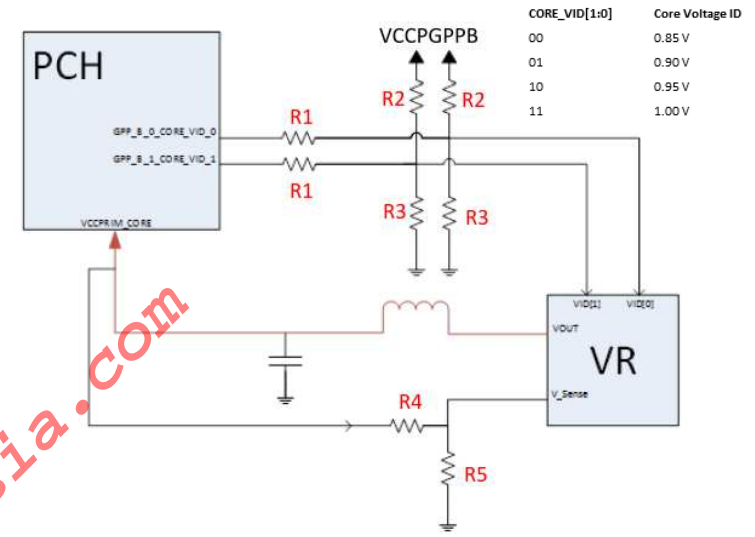
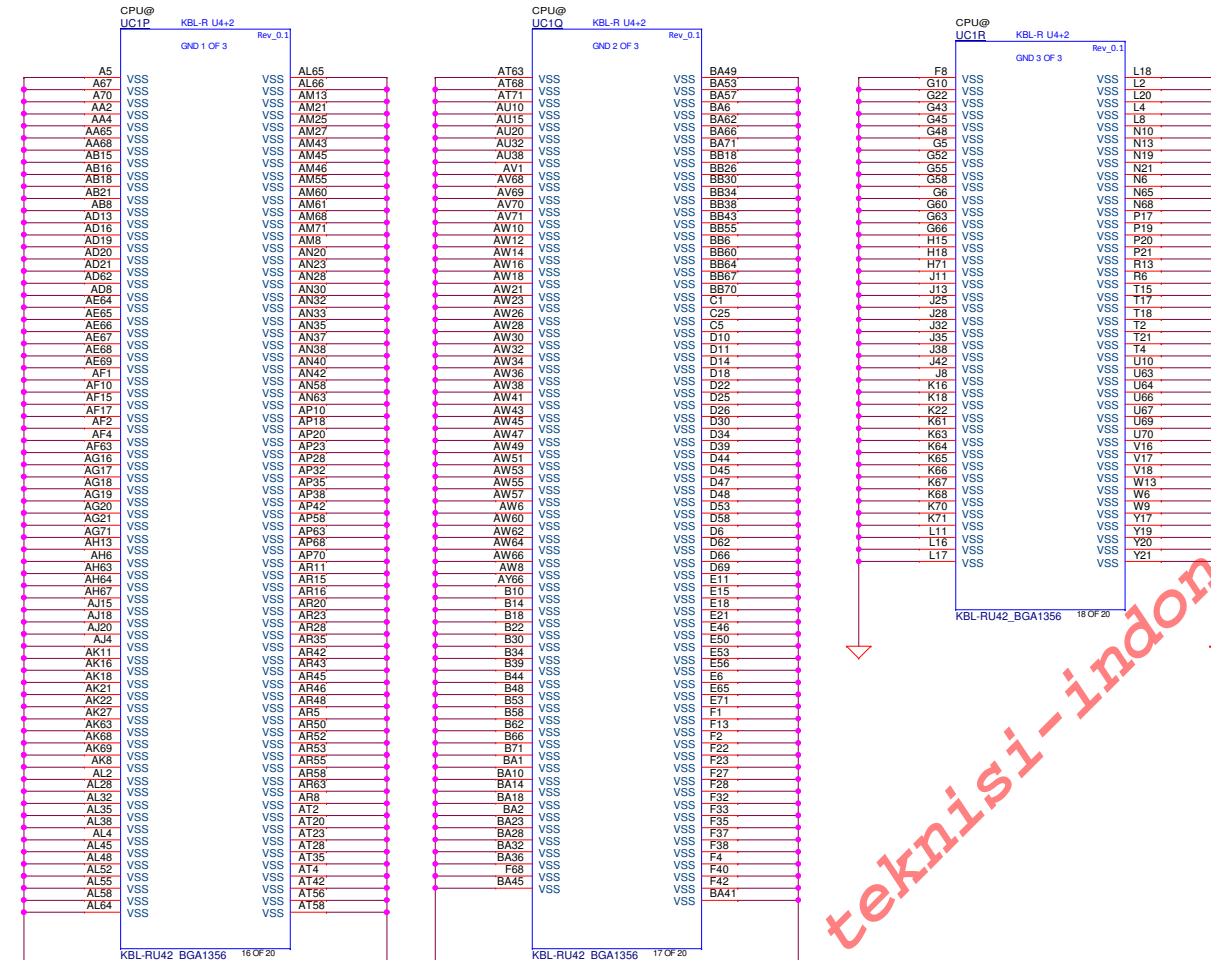
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Note1: VCCPRIM_CORE Implementat i on w t h PCH CORE_V D Reco mnendati on

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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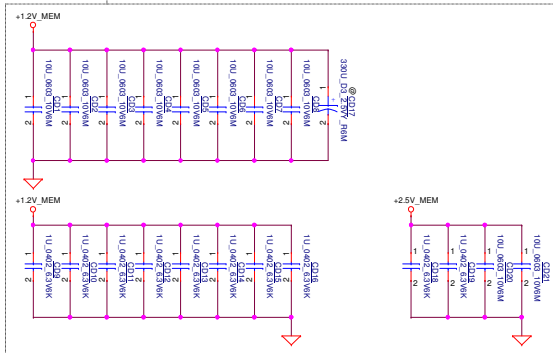


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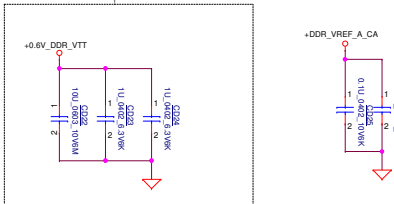
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<> DDR_A_DQS#0..7 <>>>
 <> DDR_A_DQ#0..63 <>>>
 <> DDR_A_DQS#0..7 <>>>
 <> DDR_A_MA0..16 <>>>

Layout Note:
Place near JDIMM1

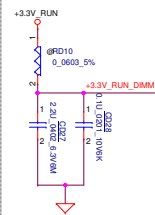
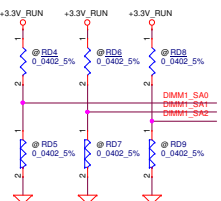


Layout Note:
Place near JDIMM1.258



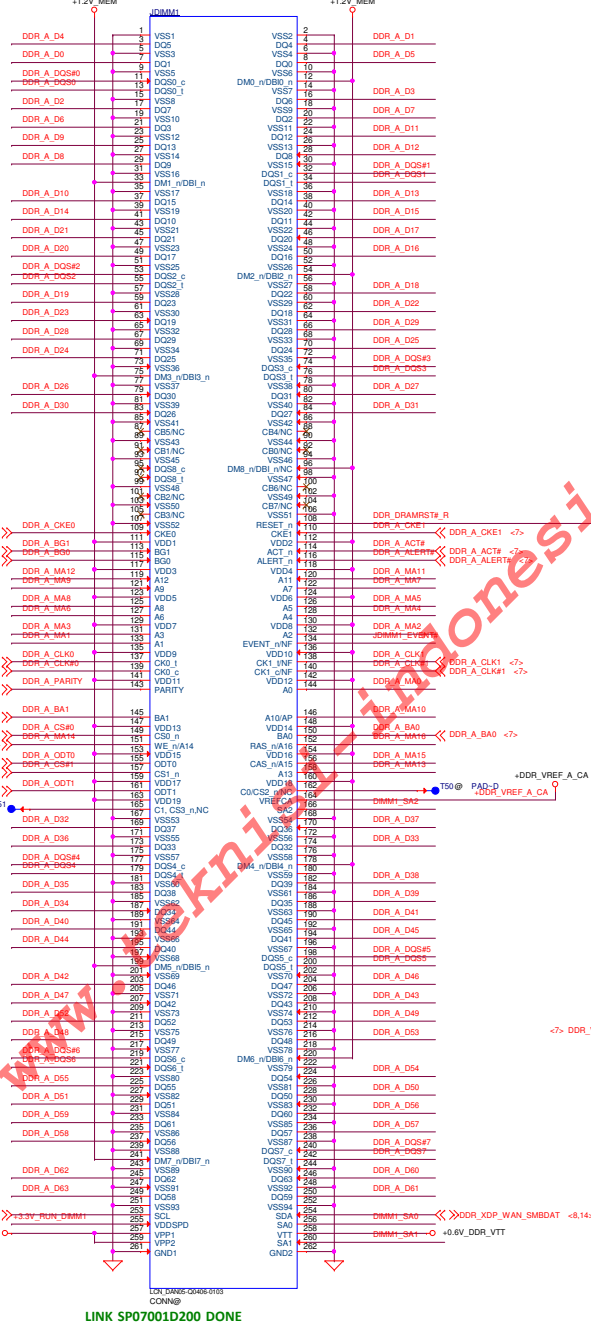
DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

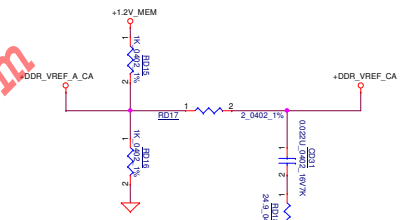
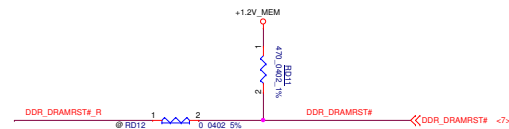


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 +2.9V_MEM

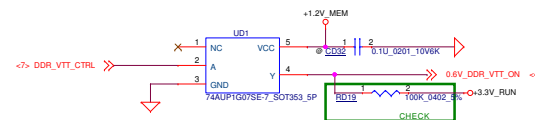
JDIMM1 REV Type H=9.2



LINK SP07001D200 DONE



JDIMM1_EVENT# <<<< H_THERMTRIP# <<12.33>>



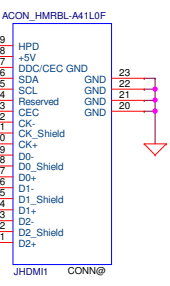
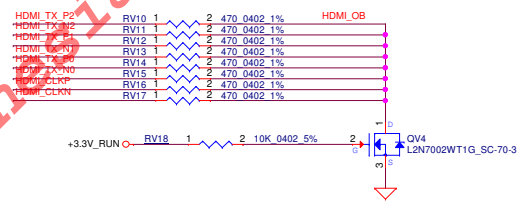
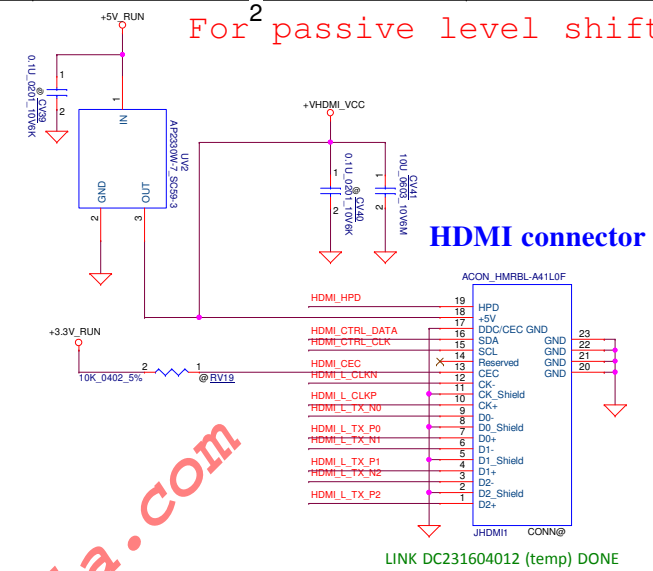
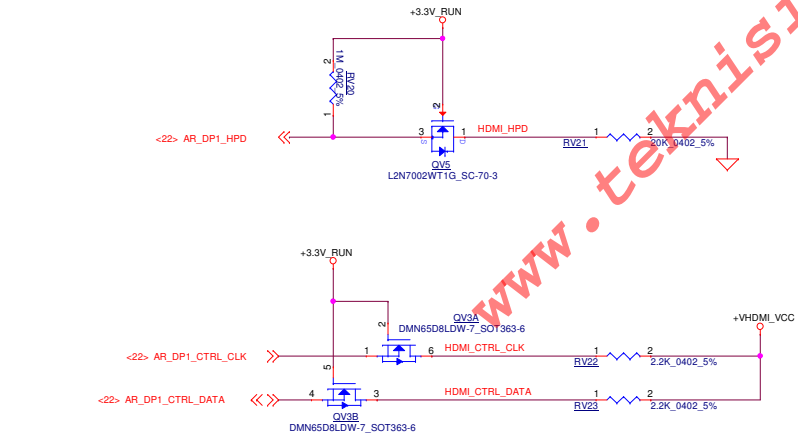
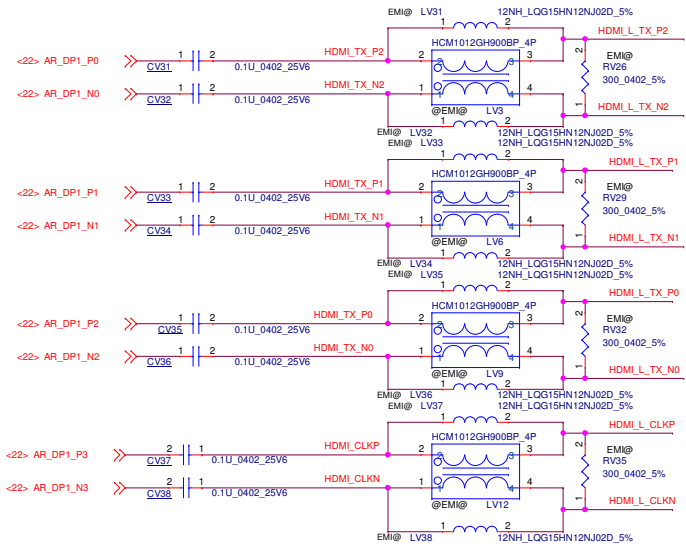
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DDR4

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HDMI CONN

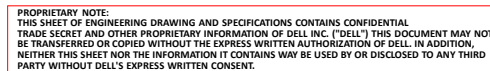
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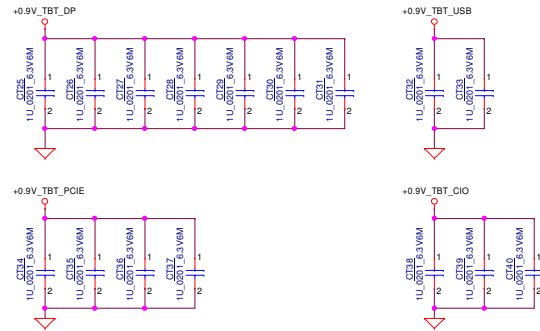
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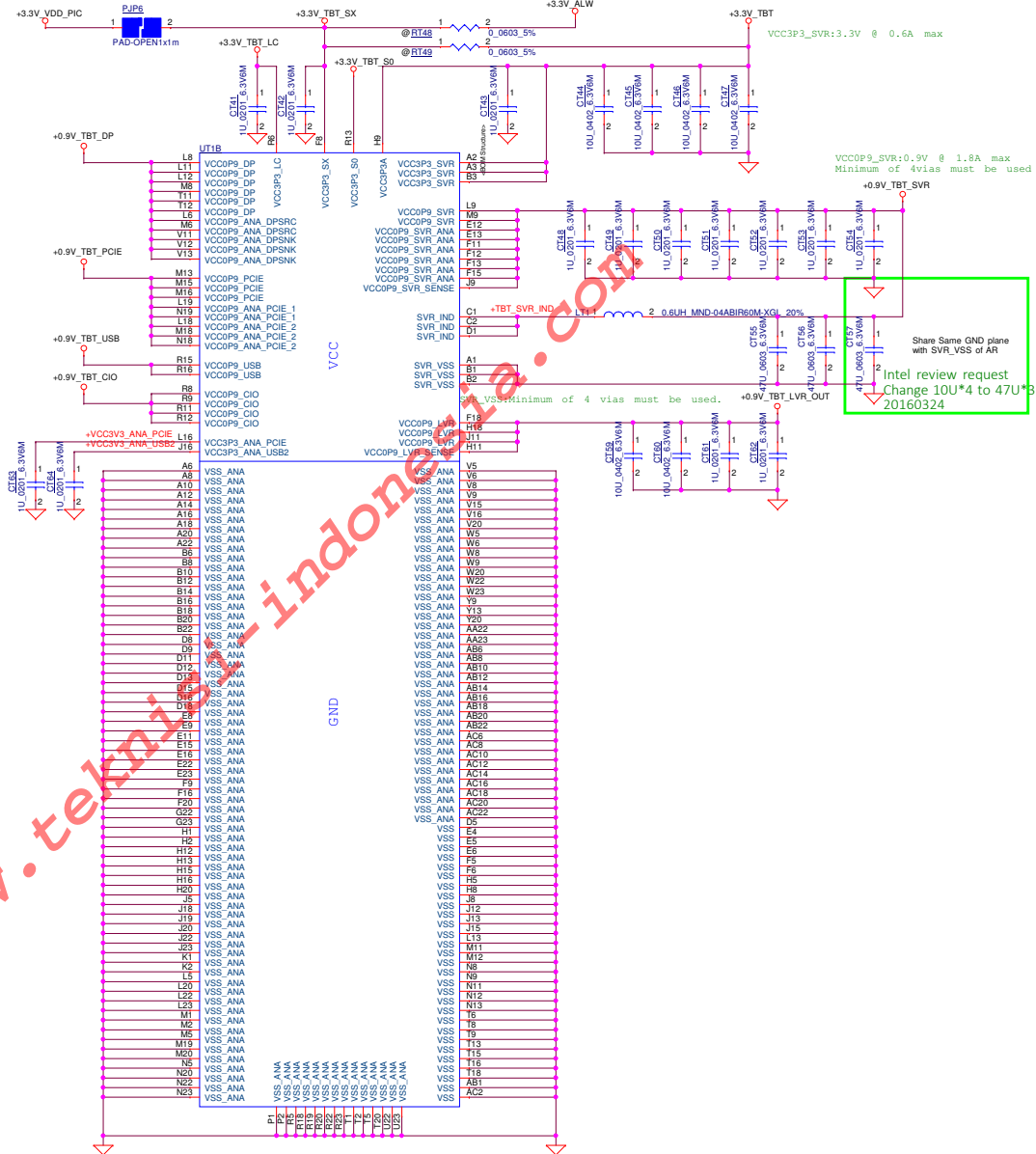
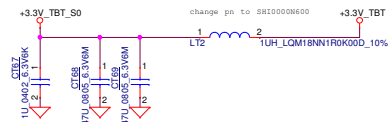
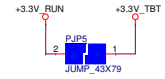


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TBT Power circuit



A16	VSS_ANA	VSS_ANA	V16
A17	VSS_ANA	VSS_ANA	V17
A18	VSS_ANA	VSS_ANA	V20
A20	VSS_ANA	VSS_ANA	V20
A22	VSS_ANA	VSS_ANA	W6
B6	VSS_ANA	VSS_ANA	W9
B8	VSS_ANA	VSS_ANA	W9
B10	VSS_ANA	VSS_ANA	W20
B12	VSS_ANA	VSS_ANA	W22
B14	VSS_ANA	VSS_ANA	W23
B16	VSS_ANA	VSS_ANA	Y9
B18	VSS_ANA	VSS_ANA	Y13
B20	VSS_ANA	VSS_ANA	Y20
B22	VSS_ANA	VSS_ANA	XA22
D6	VSS_ANA	VSS_ANA	AA23
D9	VSS_ANA	VSS_ANA	AB6
D11	VSS_ANA	VSS_ANA	AB8
D12	VSS_ANA	VSS_ANA	AB10
D18	VSS_ANA	VSS_ANA	AB12
D19	VSS_ANA	VSS_ANA	AB14
D19	VSS_ANA	VSS_ANA	AB16
D19	VSS_ANA	VSS_ANA	AB18
E8	VSS_ANA	VSS_ANA	AB20
E9	VSS_ANA	VSS_ANA	AB22
E11	VSS_ANA	VSS_ANA	AC8
E15	VSS_ANA	VSS_ANA	AC8
E16	VSS_ANA	VSS_ANA	AC10
E22	VSS_ANA	VSS_ANA	AC12
E23	VSS_ANA	VSS_ANA	AC14
F9	VSS_ANA	VSS_ANA	AC16
F16	VSS_ANA	VSS_ANA	AC18
F20	VSS_ANA	VSS_ANA	AC20
G22	VSS_ANA	VSS_ANA	AC22
G23	VSS_ANA	VSS_ANA	D6
H1	VSS_ANA	VSS_ANA	E6
H2	VSS_ANA	VSS_ANA	E8
H12	VSS_ANA	VSS_ANA	E8
H13	VSS_ANA	VSS_ANA	F6
H15	VSS_ANA	VSS_ANA	F6
H16	VSS_ANA	VSS_ANA	F6
H20	VSS_ANA	VSS_ANA	H6
J5	VSS_ANA	VSS_ANA	J8
J19	VSS_ANA	VSS_ANA	J8
J19	VSS_ANA	VSS_ANA	J8
J20	VSS_ANA	VSS_ANA	J15
J22	VSS_ANA	VSS_ANA	L13
J23	VSS_ANA	VSS_ANA	M11
K1	VSS_ANA	VSS_ANA	M12
K2	VSS_ANA	VSS_ANA	VSS

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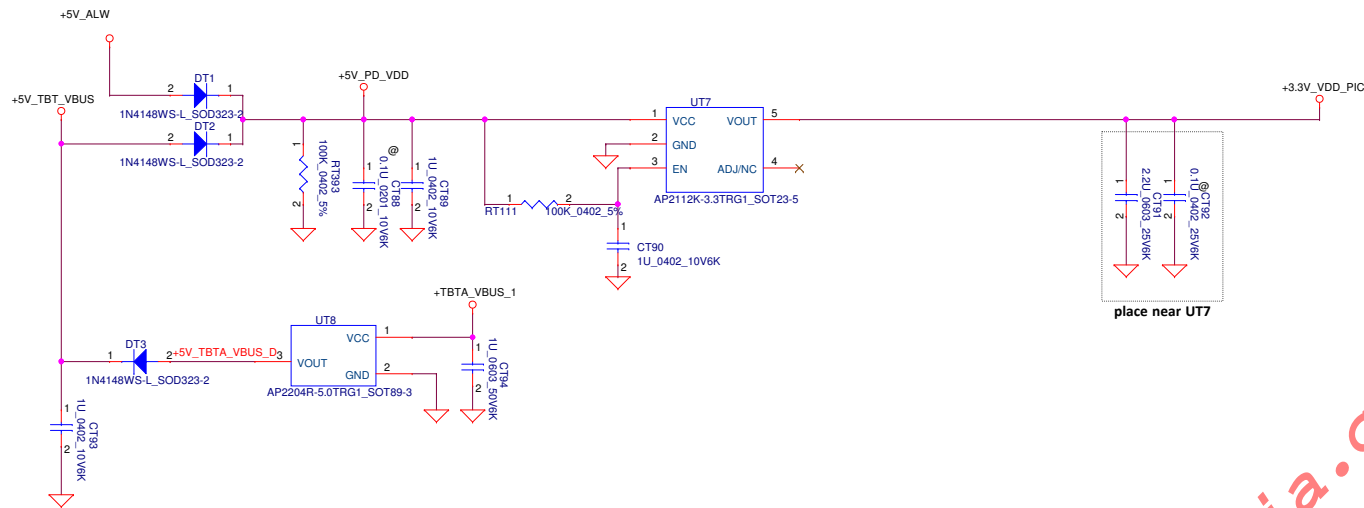
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Title **TBT-AR-SP(2/2) PWR,VSS**

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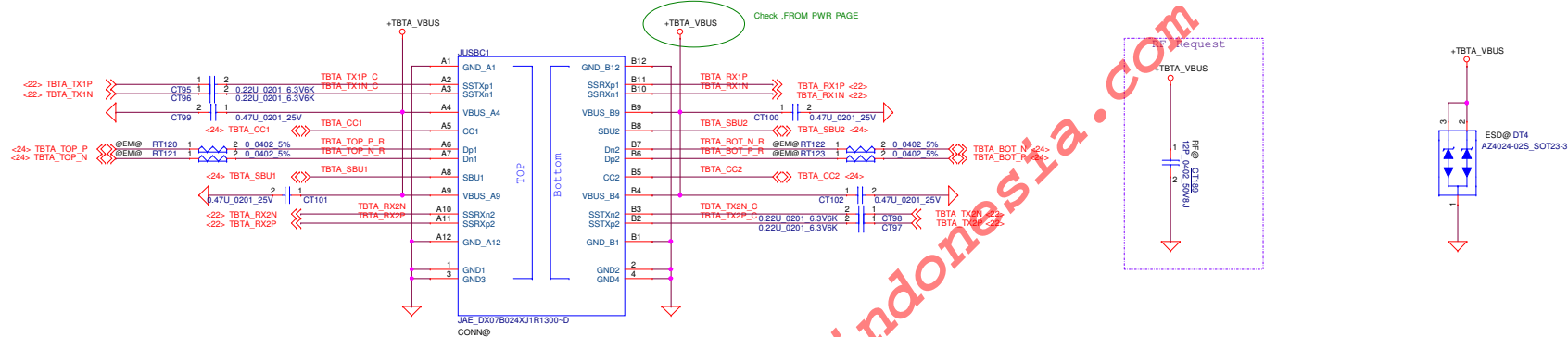
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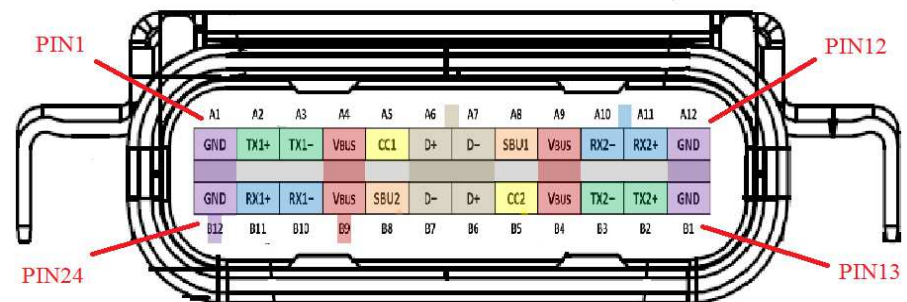
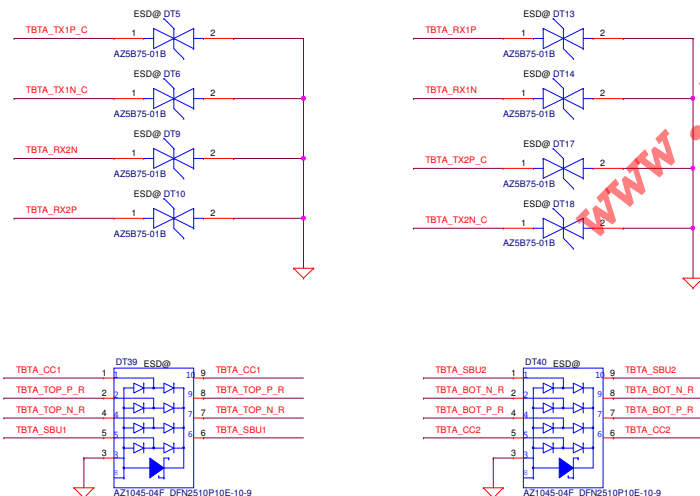
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Title			[Type C]PD Power	
Size			Document Number	Rev
			LA-F311P	2.0
Date:			Wednesday, December 20, 2017	Sheet 25 of 58

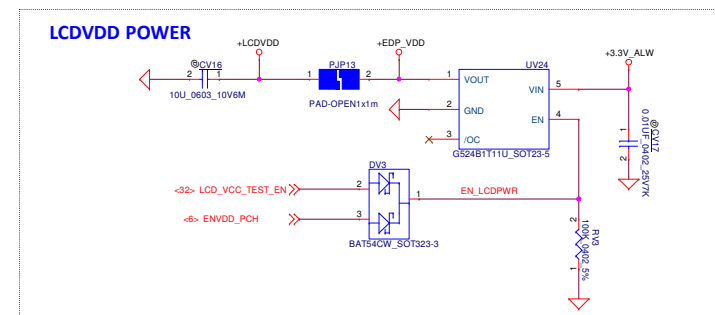
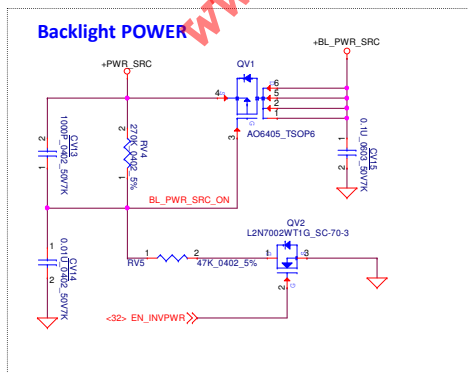
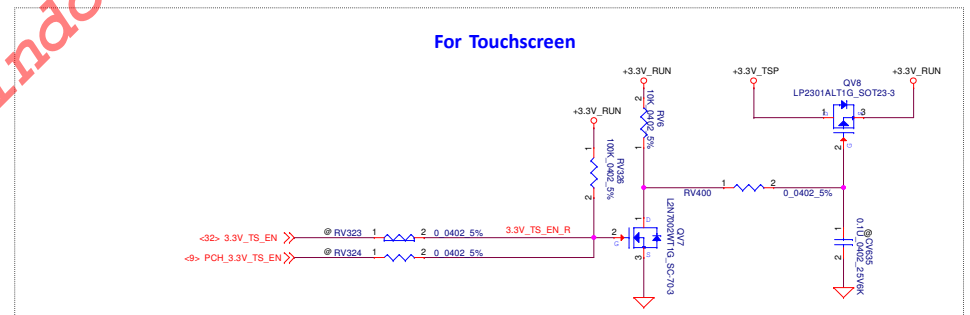
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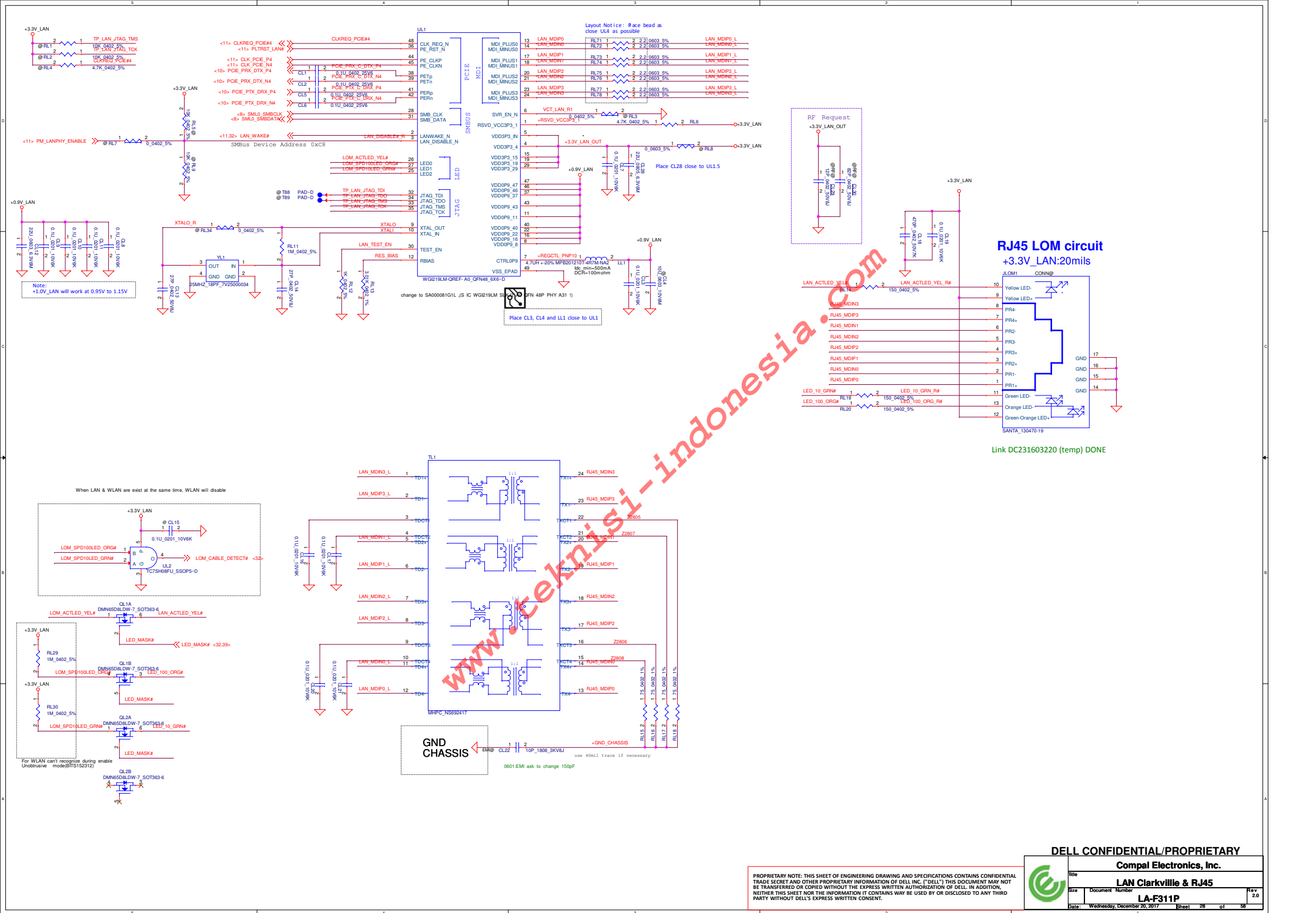


```
Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B
Link DC23300MEBL Done
```

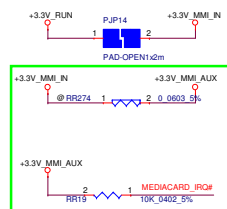
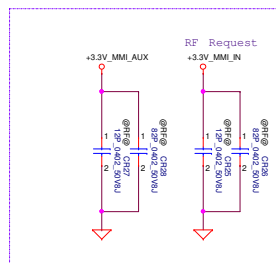


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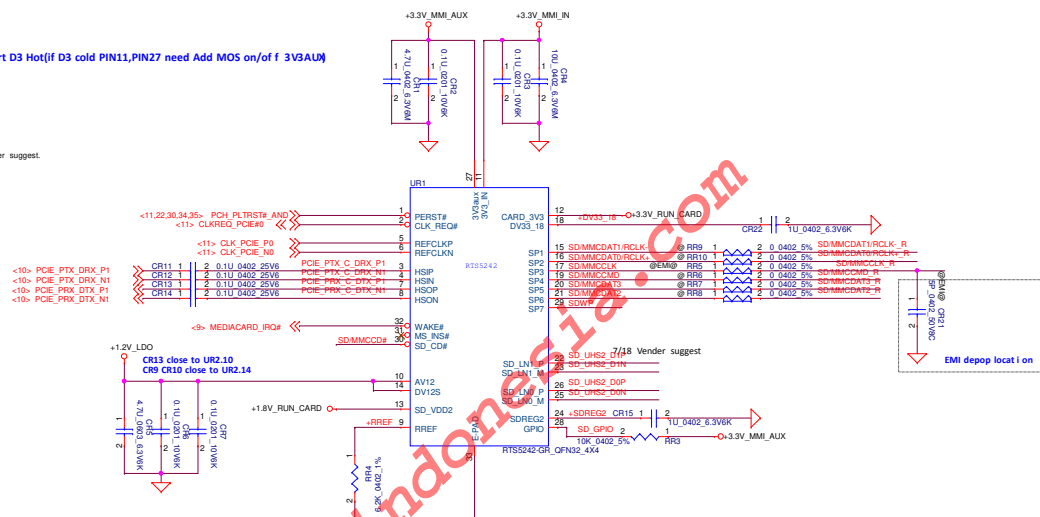


For PCIe Interface

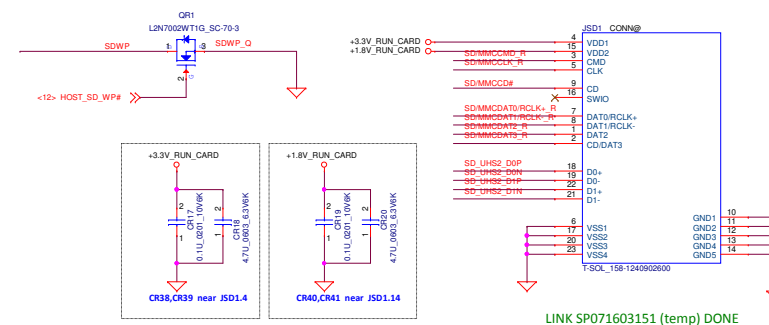


support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/of f 3V3AUX)

7/18 Vender suggest.



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	Low	Low	Write Enable
Low	Low	High	Write Protect(FW LOCK)



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Card Reader RTS5242

LA-F311P

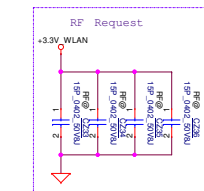
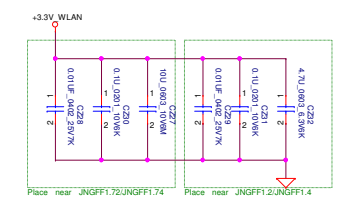
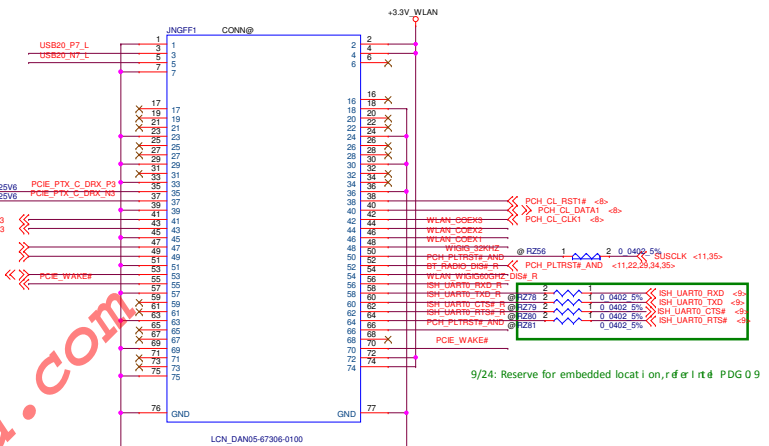
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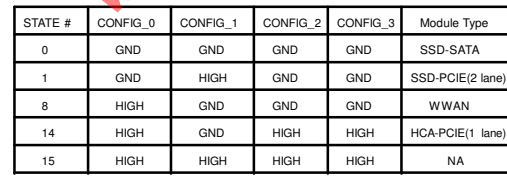


for AR Steamboat

NGFF slot B Key B



SIM Card Push-Push



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIe(2 lane)
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIe(1 lane)
15	HIGH	HIGH	HIGH	HIGH	NA

Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

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NGFF Card

LA-F311P

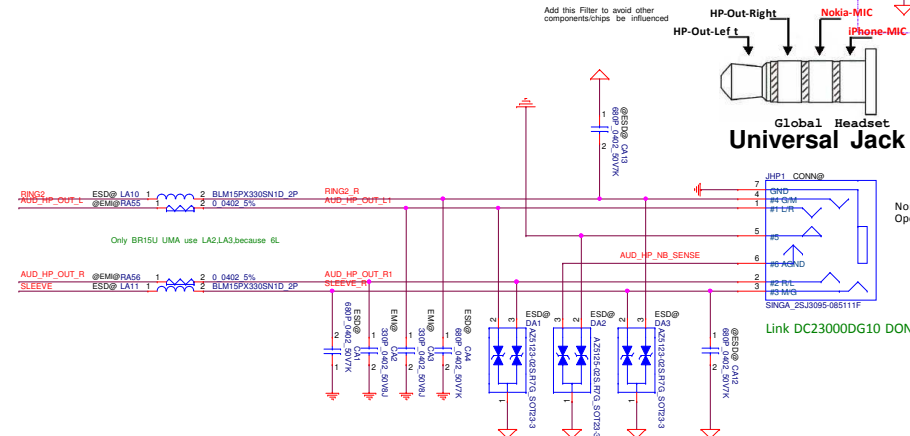
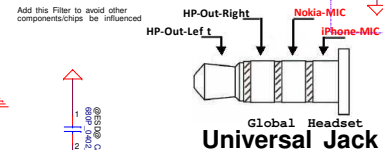
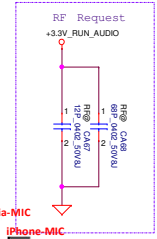
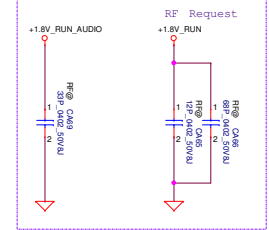
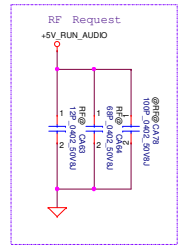
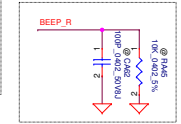
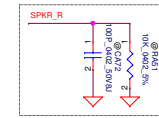
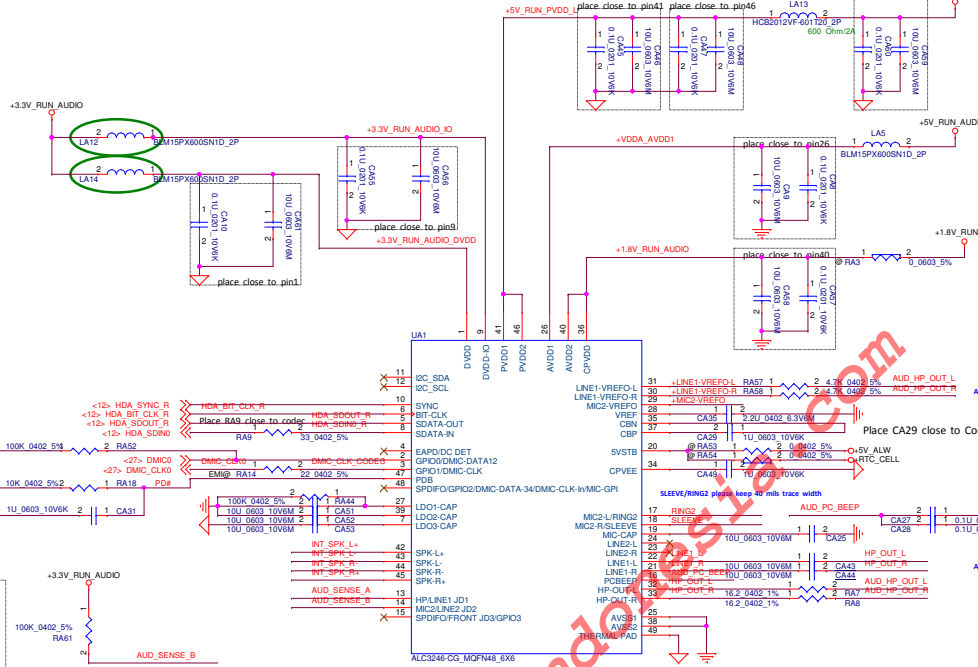
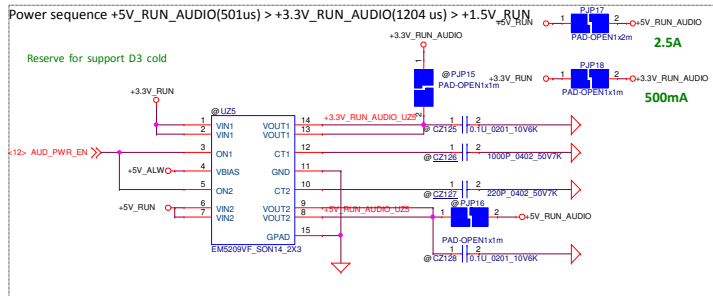
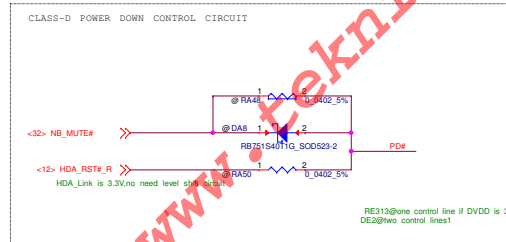
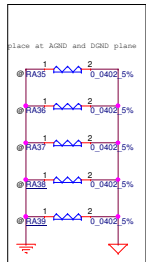
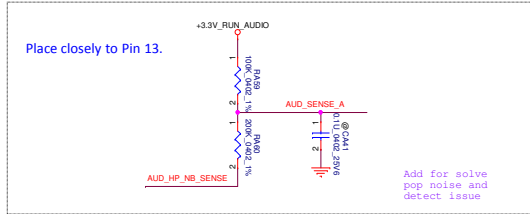
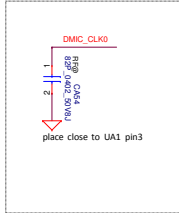
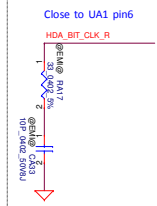
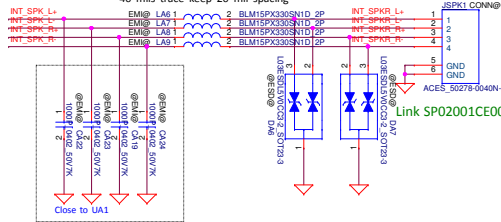
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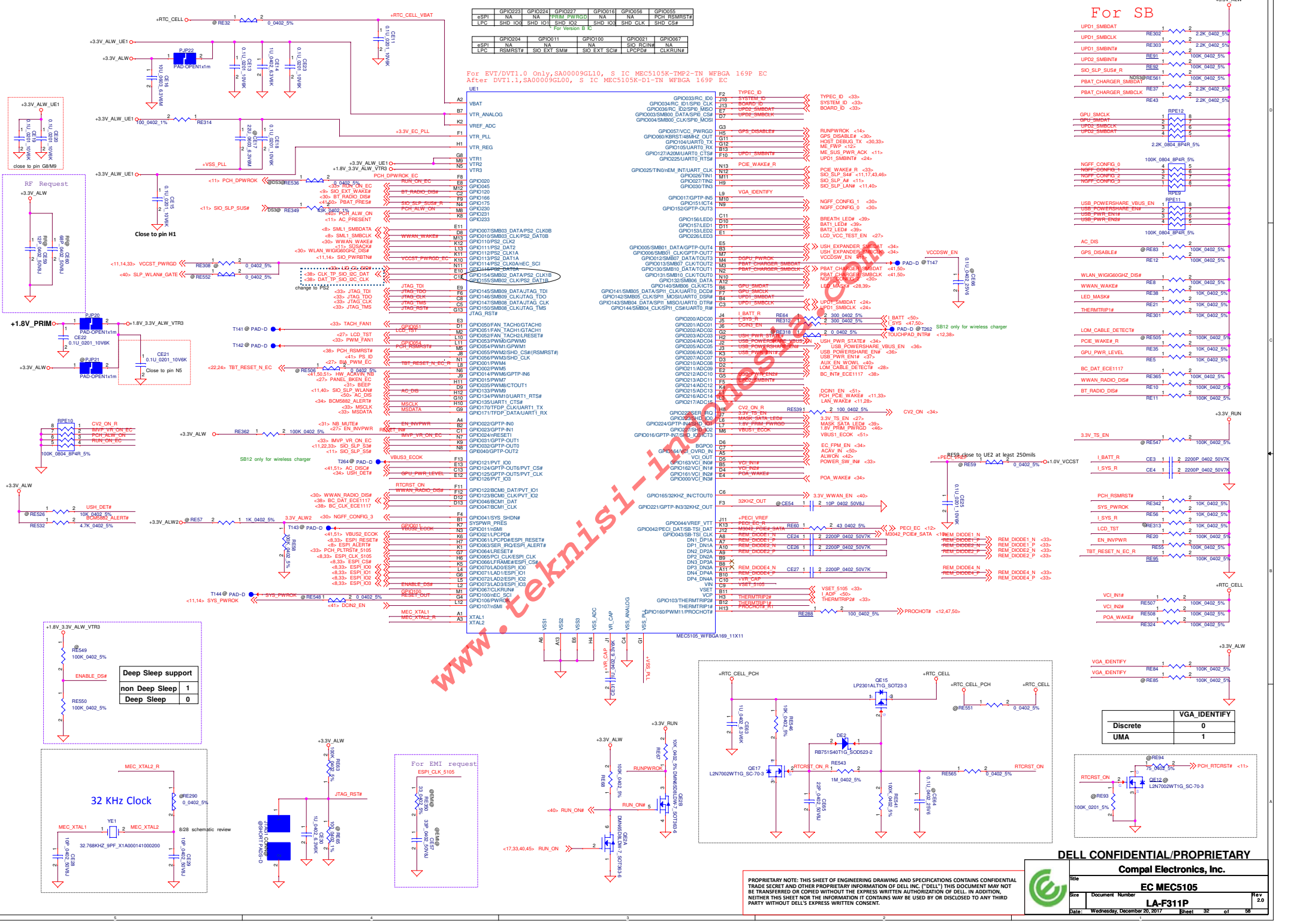
1W x 1ch, 4ohm (Transducer spec is 8Ohm0.5Watt per unit, there are two transducer units in one speaker box)

Internal Speakers Header

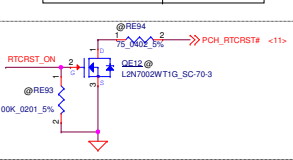
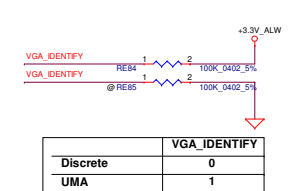
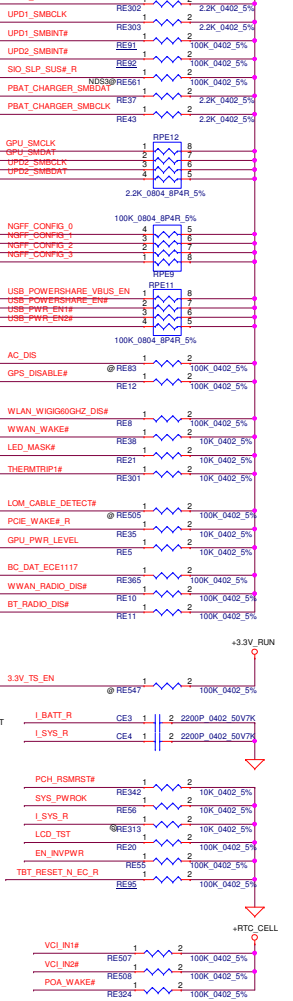
40 mils trace keep 20 mil spacing



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For SB

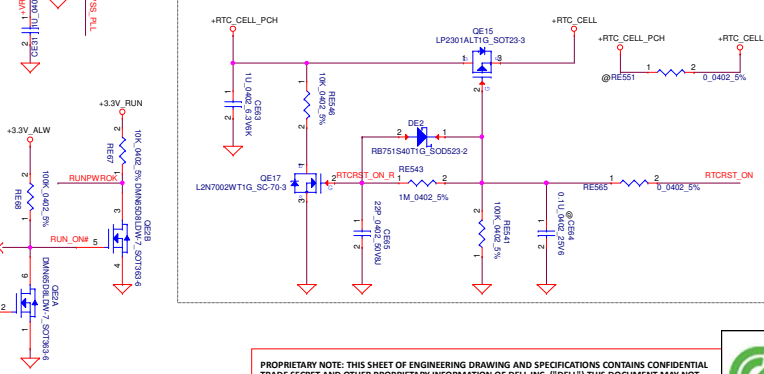
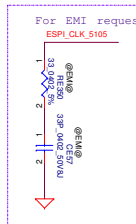


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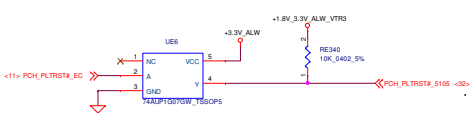
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Deep Sleep support	
non Deep Sleep	1
Deep Sleep	0

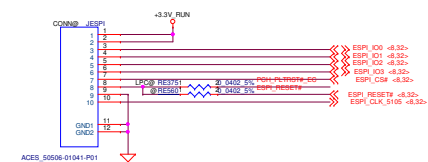
32 KHz Clock



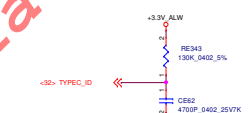
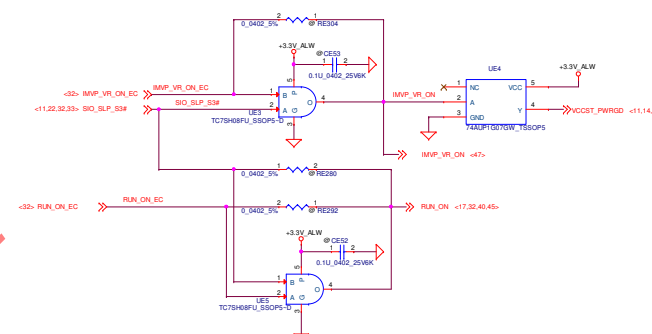
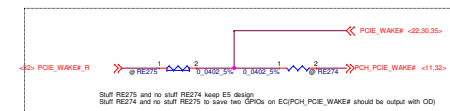
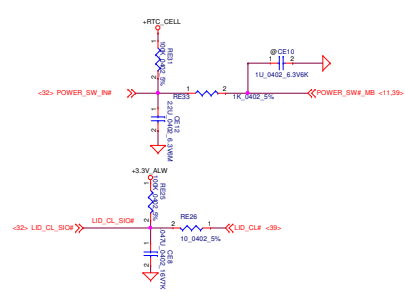
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PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	



LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_I00
4	LPC_LAD1	ESPI_I01
5	LPC_LAD2	ESPI_I02
6	LPC_LAD3	ESPI_I03
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK



RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	.
2K	4700p	.
1K	4700p	.

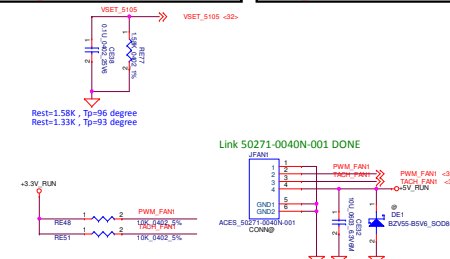
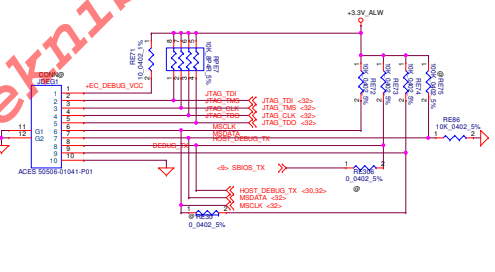
RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
4.3K	4700p	A00
2K	4700p	A01
1K	4700p	.

RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
33K	4700p	14"
8.2K	4700p	15"
4.3K	4700p	17"
2K	4700p	15P
1K	4700p	.

PD ACE_DET# rise t_i n_is measured from m5 %68 %

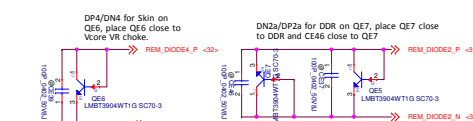
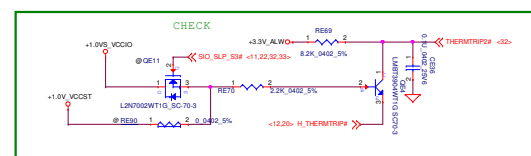
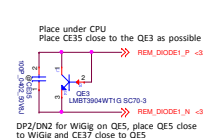
BOARD ID rise t_i n_is measured from m5 %68 %

SYSTEM ID rise t_i n_is measured from m5 %68 %



Thermal diode mapping

5105 Channel	Locat i on
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

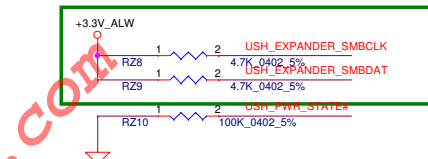


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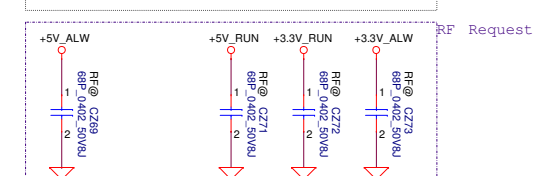
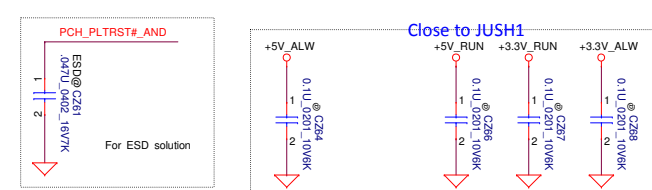
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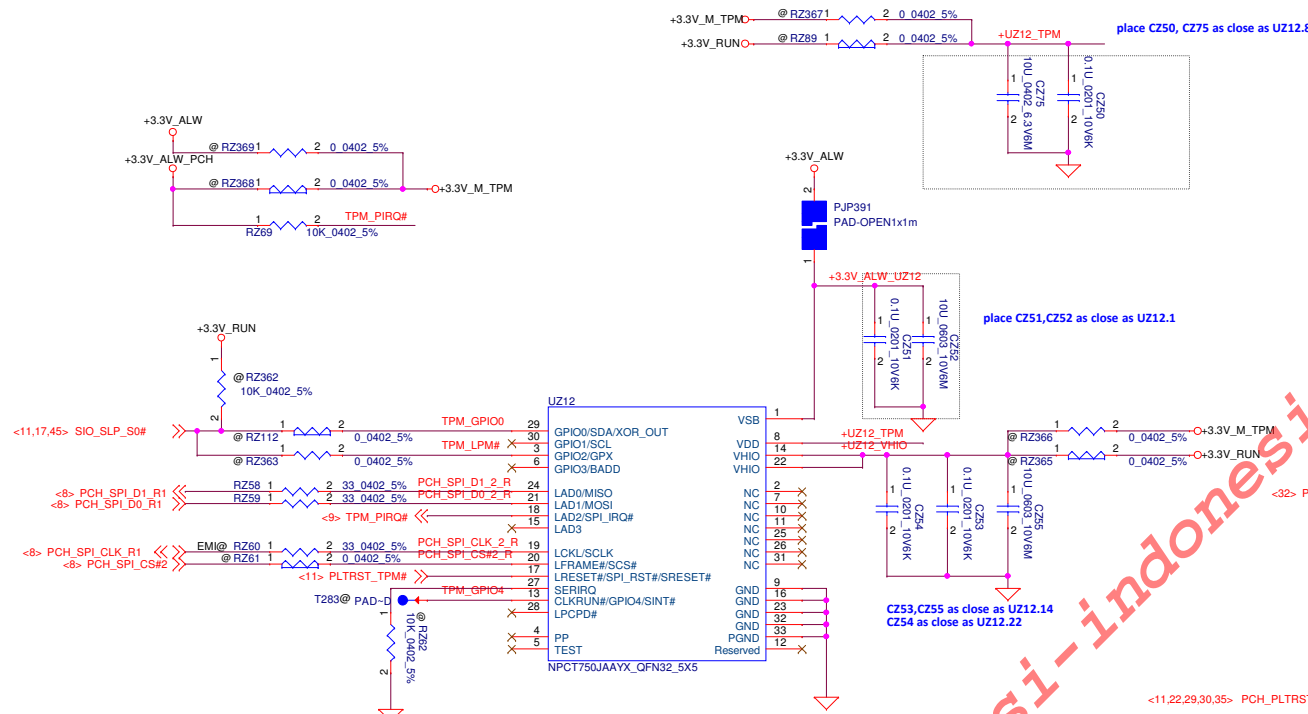
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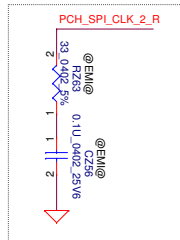
USH & TPM

LA-E311P

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	Pop	Depop	Comment
NPCT65x	RZ89, RZ366, RZ62, RZ363	RZ365, RZ367, RZ112	VDD - V ₁ RUN Power VIO - V ₁ SPI Power
NPCT75x	RZ89, RZ365, RZ112	RZ367, RZ366, RZ62, RZ363	Option1 (recommended) VDD and VHIO - V ₁ RUN power
NPCT75x	RZ367, RZ366	RZ89, RZ365, RZ62	Option2 (for Z1 sample [early sample]) VDD and VHIO - V ₁ SPI power

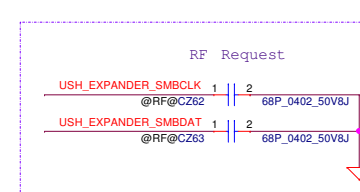


PCH_PLTRST#_AND

ESD@C261
.047U .0402 .16V7K

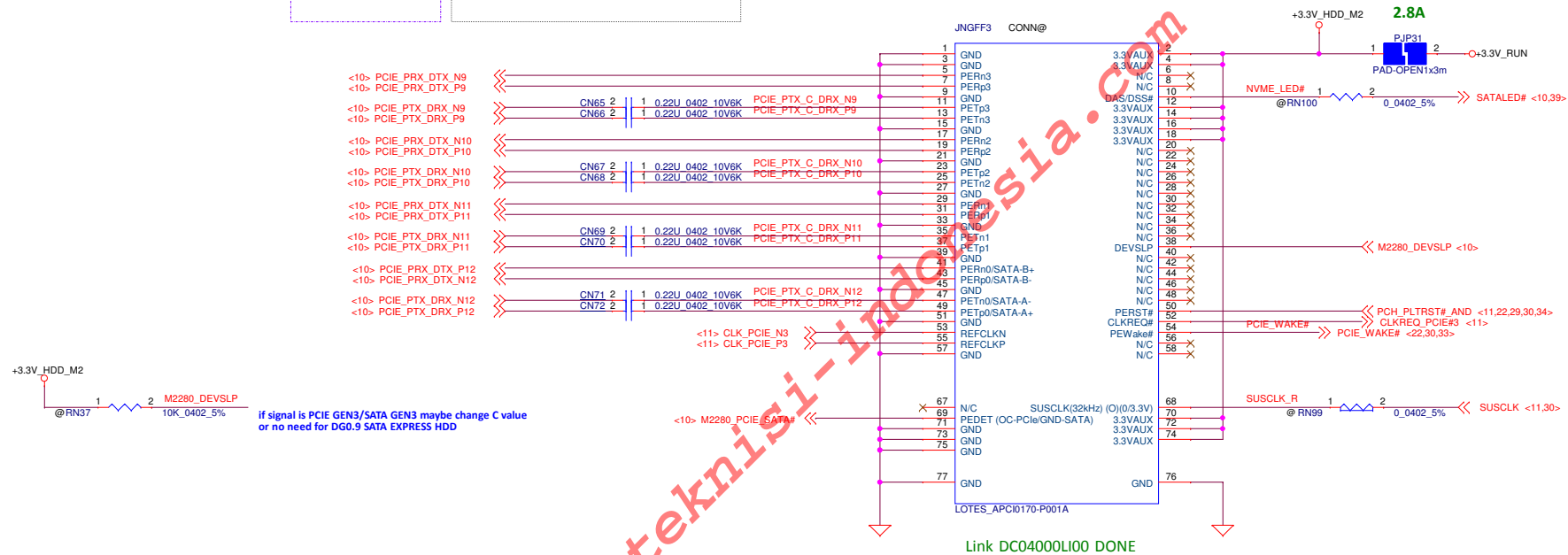
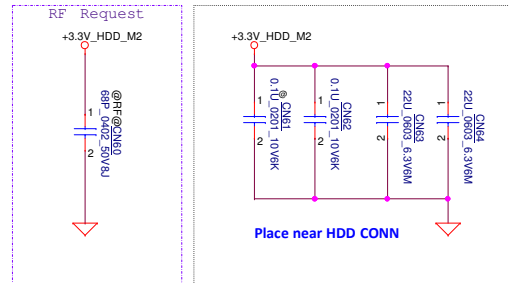
1 2

For ESD solution



2280 SSD

NGFF slot C Key M



Link DC04000LI00 DONE

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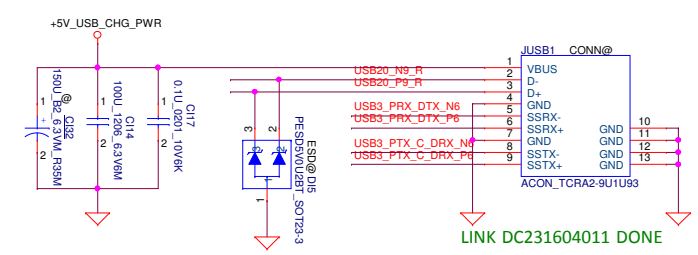
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M2 2280 Socket

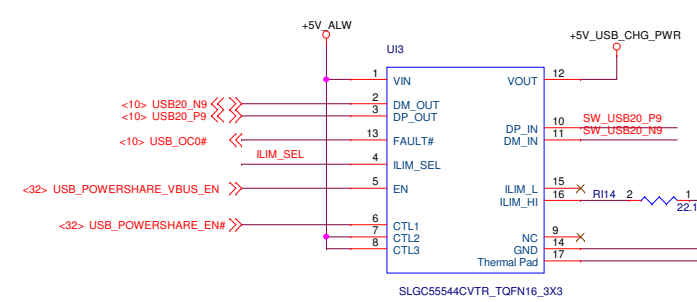
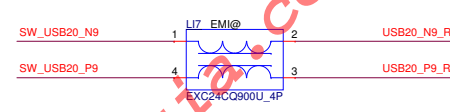
LA-F311P

2.0

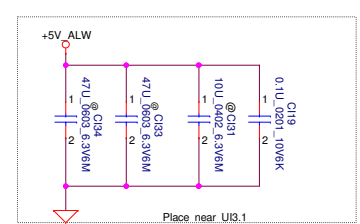
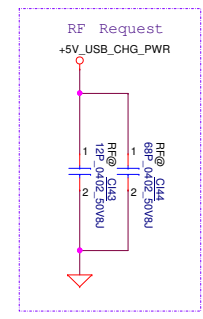
Date: Wednesday, December 20, 2017 Sheet 35 of 58



LINK DC231604011 DONE



SA000097E10 Link Done



Place near UI3.1

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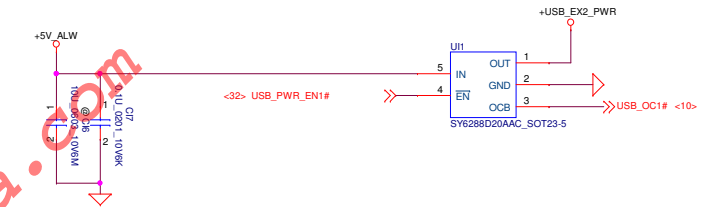
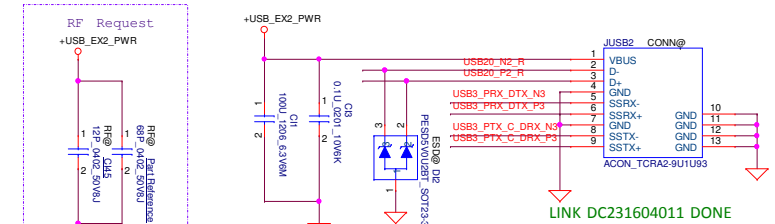
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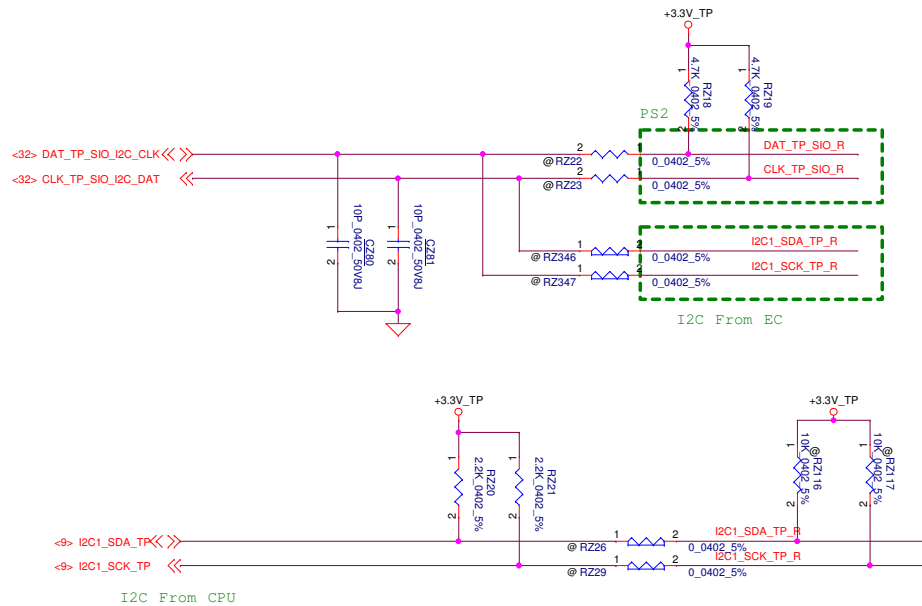
Title		
JUSB1+PS		
Size	Document Number	Rev
	LA-F311P	2.0
Date:	Wednesday, December 20, 2017	Sheet 36 of 58

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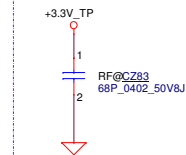
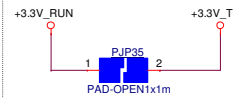


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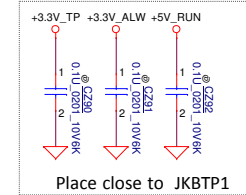
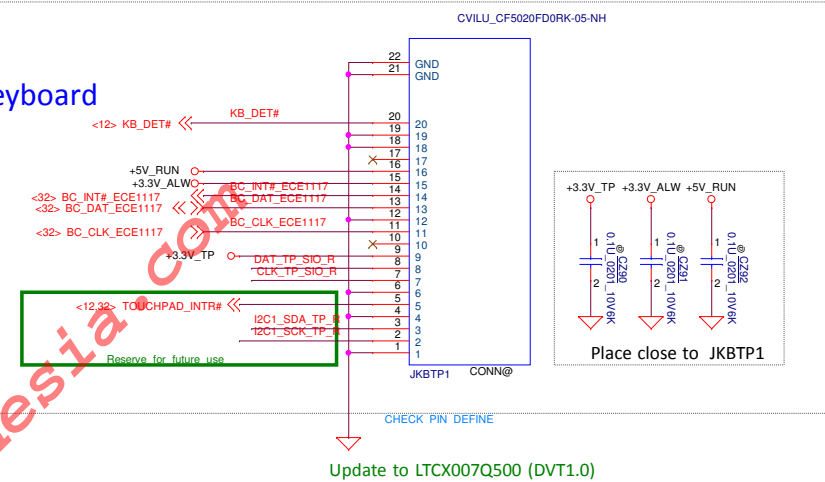
Touch Pad



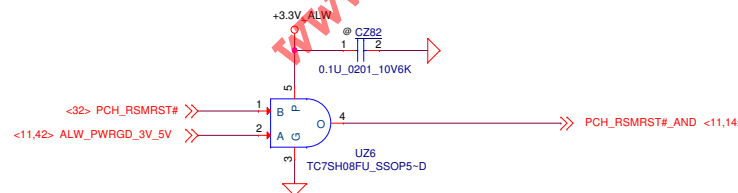
Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues



Keyboard



RSMRST circuit



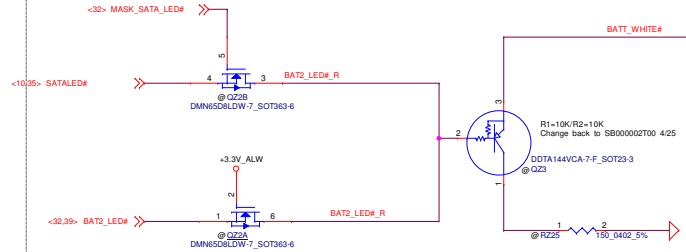
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Title			
Keyboard			
Size	Document Number	Rev	
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HDD LED MUX

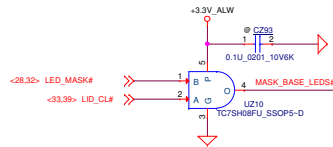
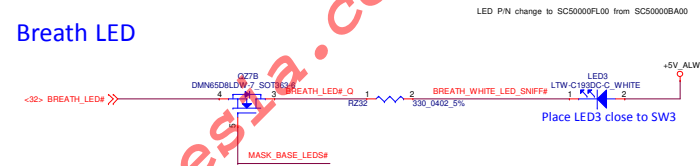
means EC can switch battery white led and HDD LED by hot key "Fn+H"



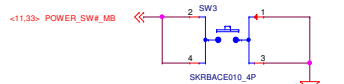
Battery LED



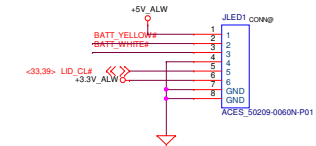
Breath LED



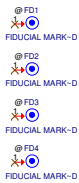
POWER & INSTANT ON SWITCH



LED board CONN

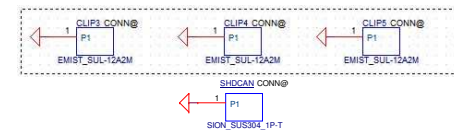
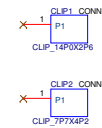
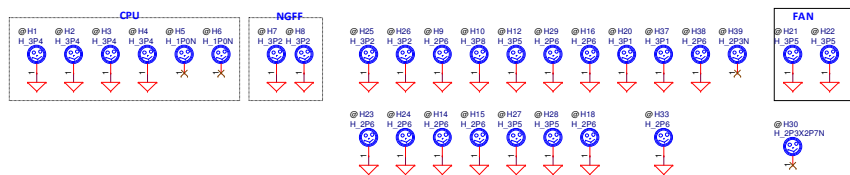


Fiducial Mark



LED Circuit Control Table

	LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



Shielding can clip no pop no footprint, just reserve for schematic.

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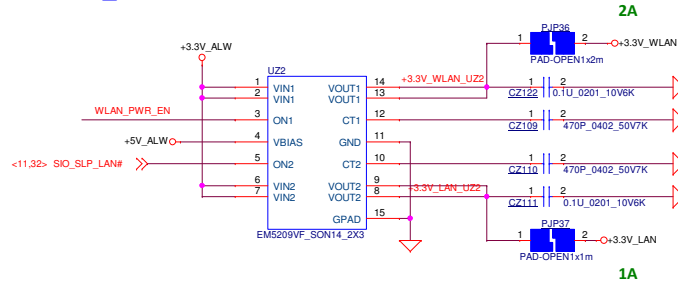
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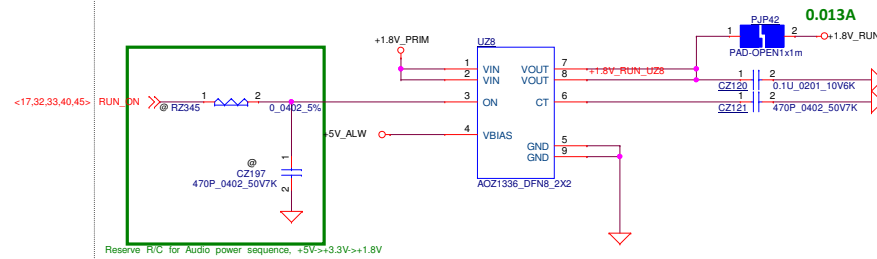
PAD, LED		
Rev	2.0	
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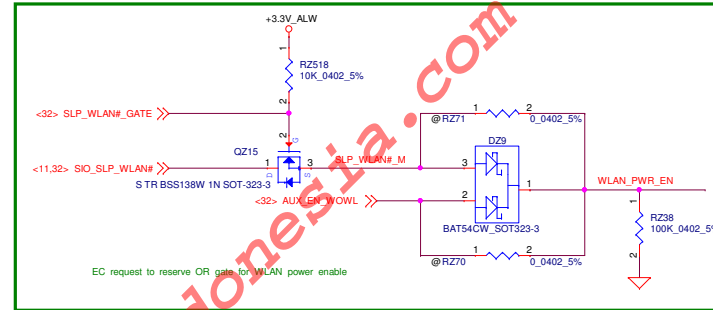
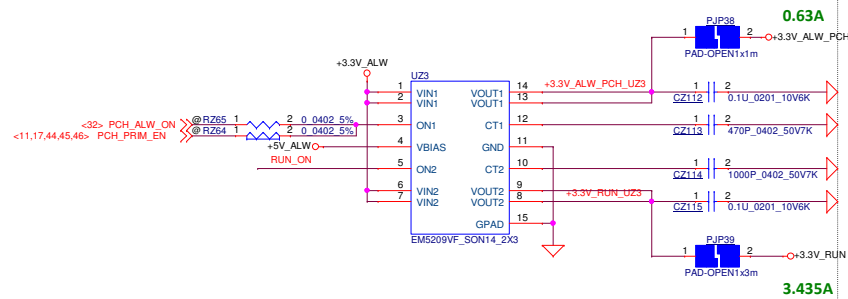
+3.3V_WLAN/+3.3V_LAN source



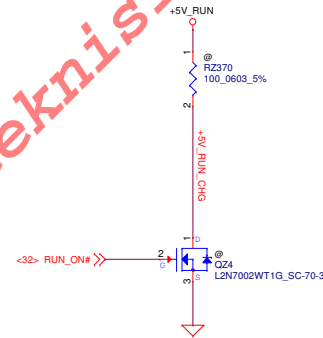
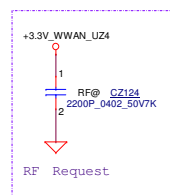
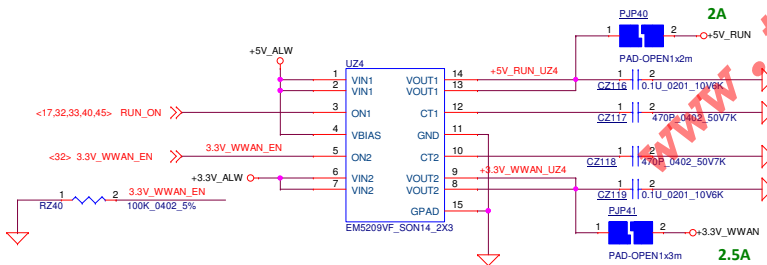
+1.8V_RUN source



+3.3V_ALW_PCH/+3.3V_RUN source



+5V_RUN/+3.3V_WWAN source



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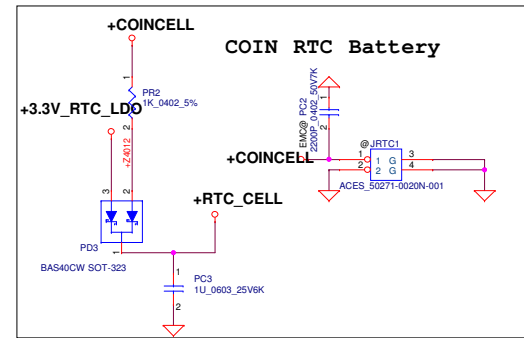
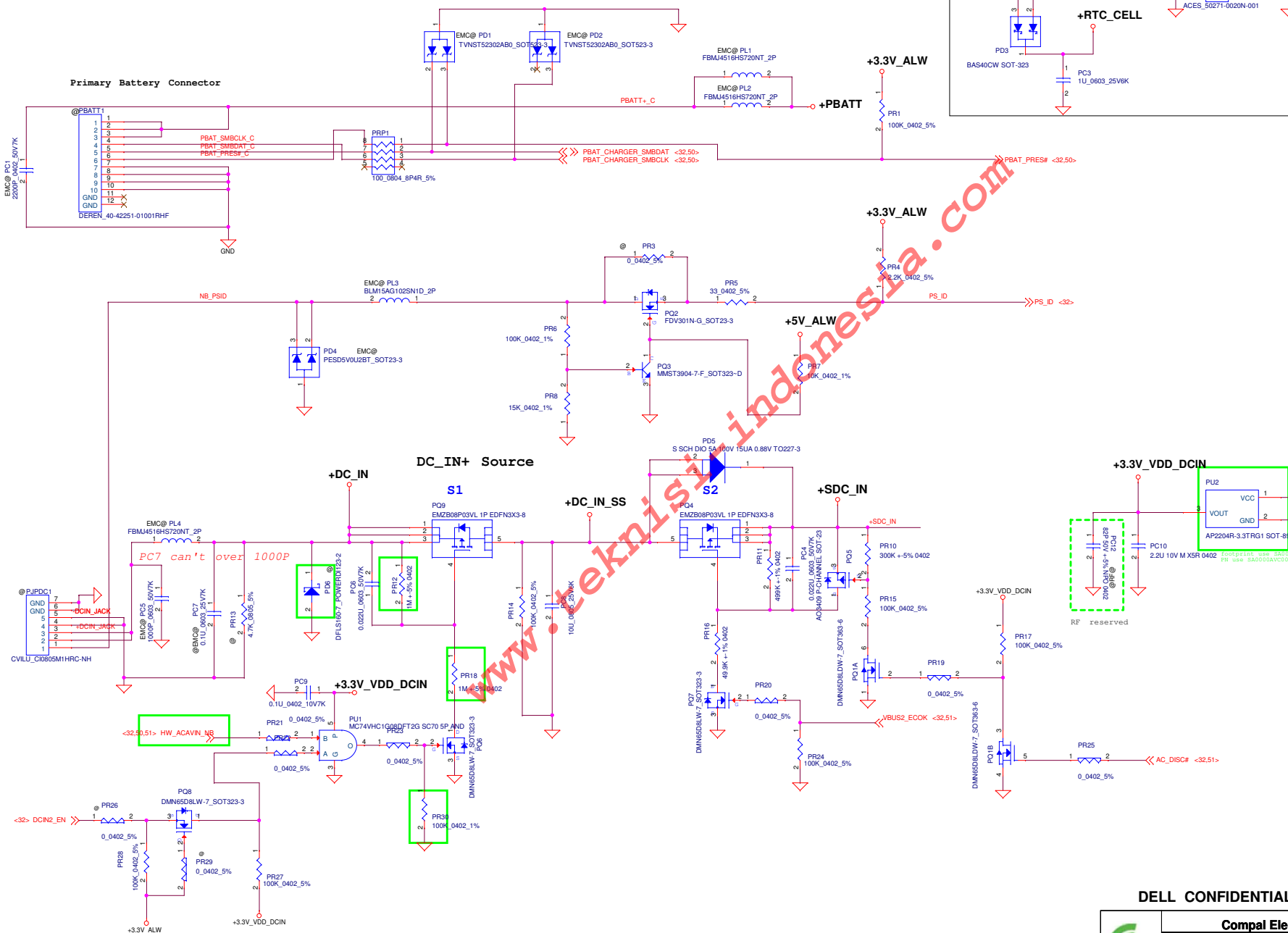
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Power control

LA-F311P

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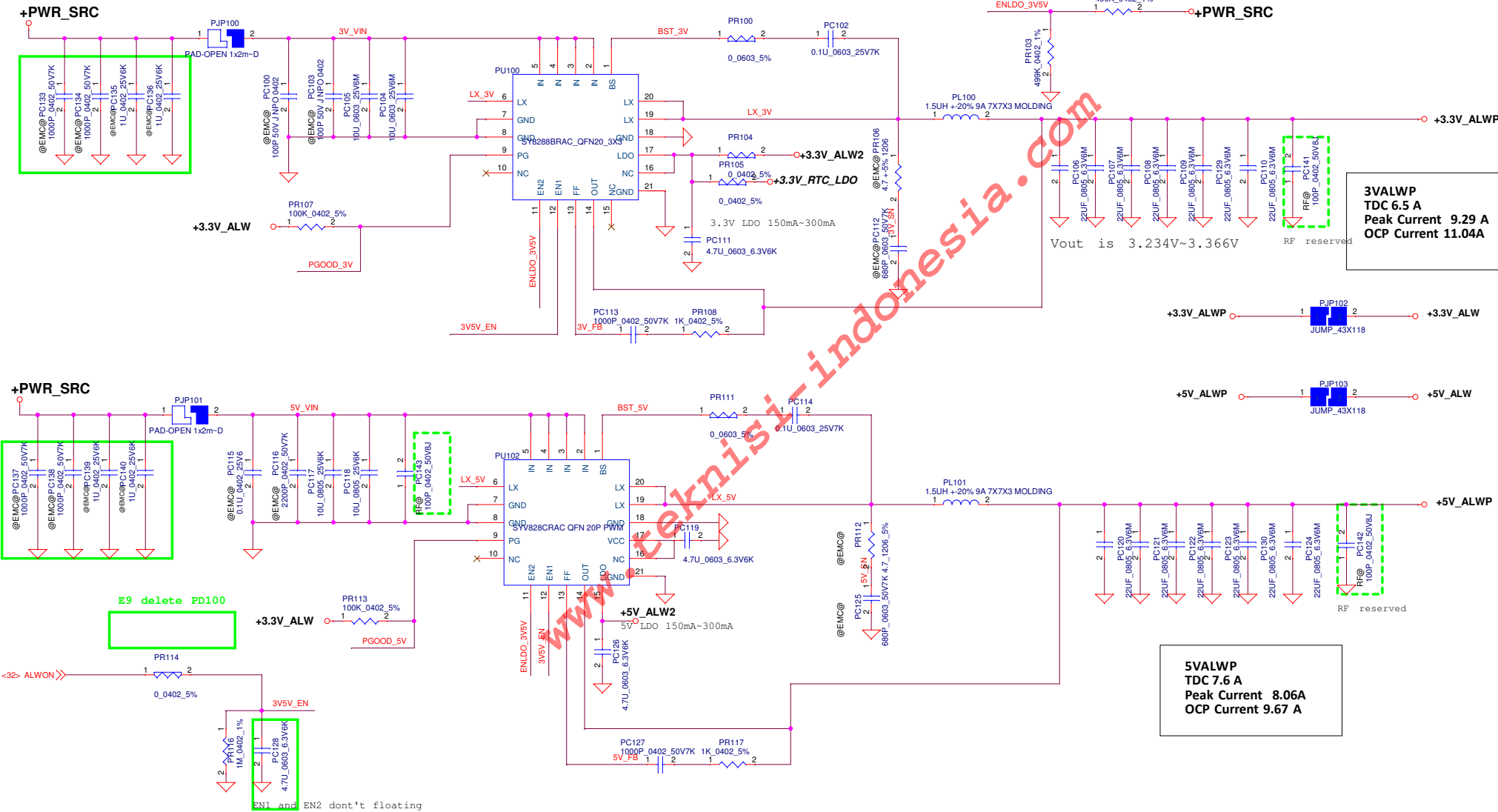
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		+DCIN	
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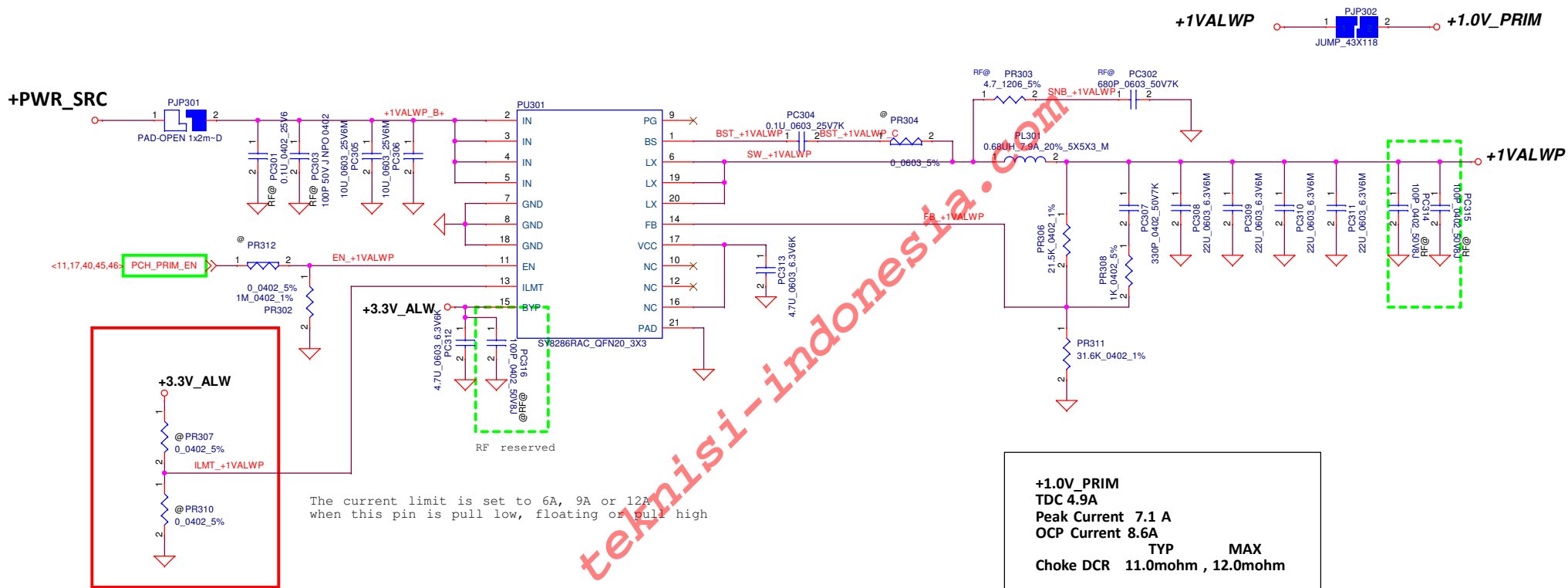
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Title		+5V_ALW/3.3V_ALW	
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		Rev	2.0



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Title	+1VALWP	
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Local sense put on HW site

+1.0V_VCCST

VCC_SA U22
TDC 4.0A
Peak Current 4.5A
OCP current 10A
Choke DCR 6.2 m ohm

VCC_SA U42
TDC 4.0A
Peak Current 5A
OCP current 10A
Choke DCR 6.2 m ohm

VCCSA_B+ CPU_B+

VCCSA_B+

+VCC_SA

+5V_ALW

+5V_ALW

<16> VCC_GT_SENSE

<16> VSS_GT_SENSE

Local sense put on HW site

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PWR_VCORE_ISL95857

LA-F311P

Rev 2.0

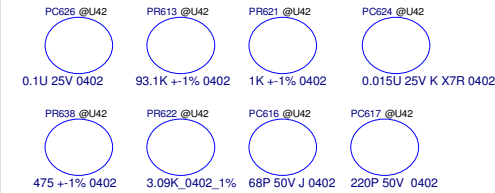
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VCC_core (U22)
TDC 21A
Peak Current 32A
OCP current 38.4A
Choke DCR 0.9 +-5% ohm

VCC_core (U42)
TDC 42A
Peak Current 64A
OCP current 76.8A
Choke DCR 0.9 +-5% ohm

U42

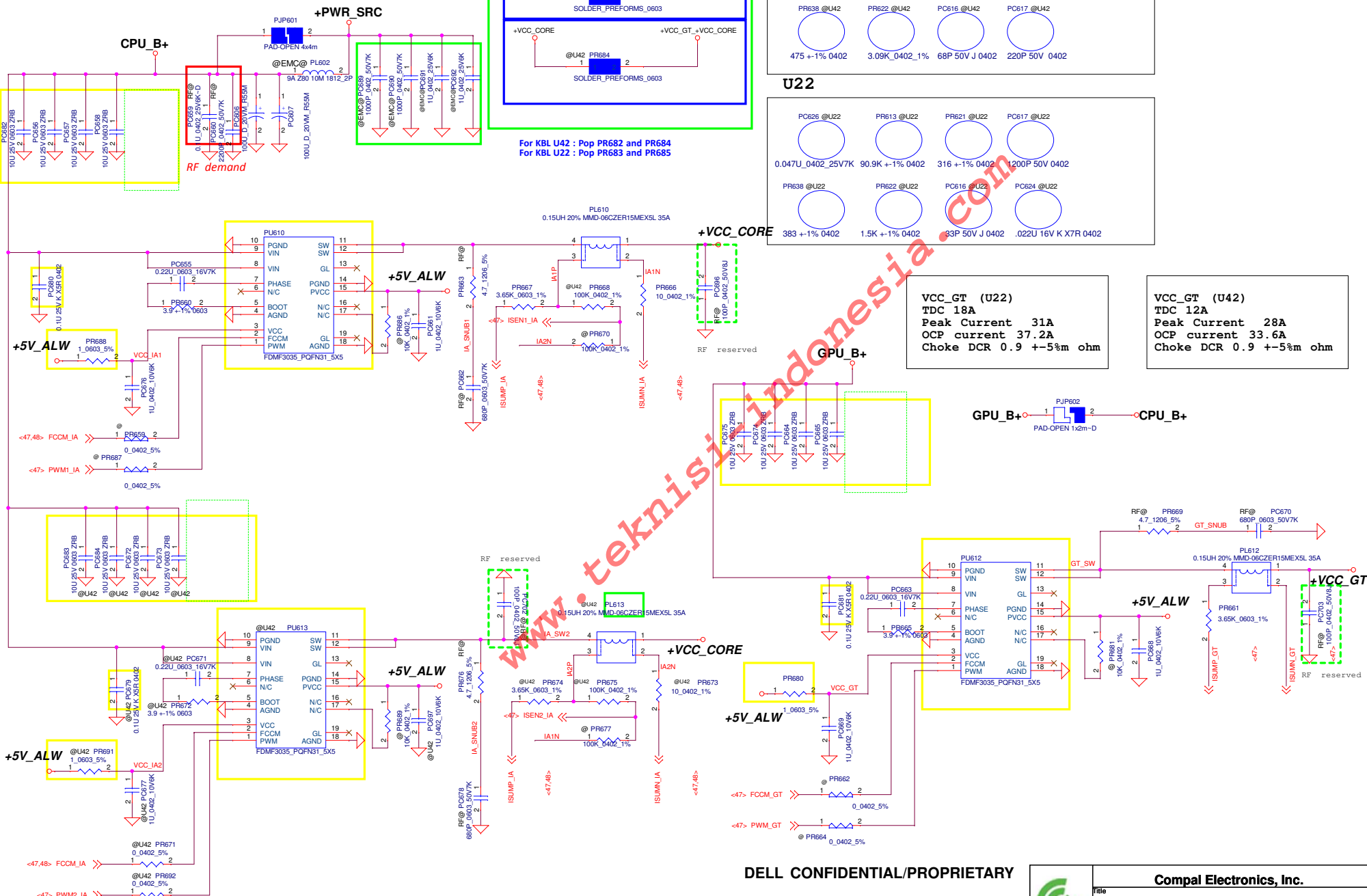


U22



VCC_GT (U22)
TDC 18A
Peak Current 31A
OCP current 37.2A
Choke DCR 0.9 +-5% ohm

VCC_GT (U42)
TDC 12A
Peak Current 28A
OCP current 33.6A
Choke DCR 0.9 +-5% ohm



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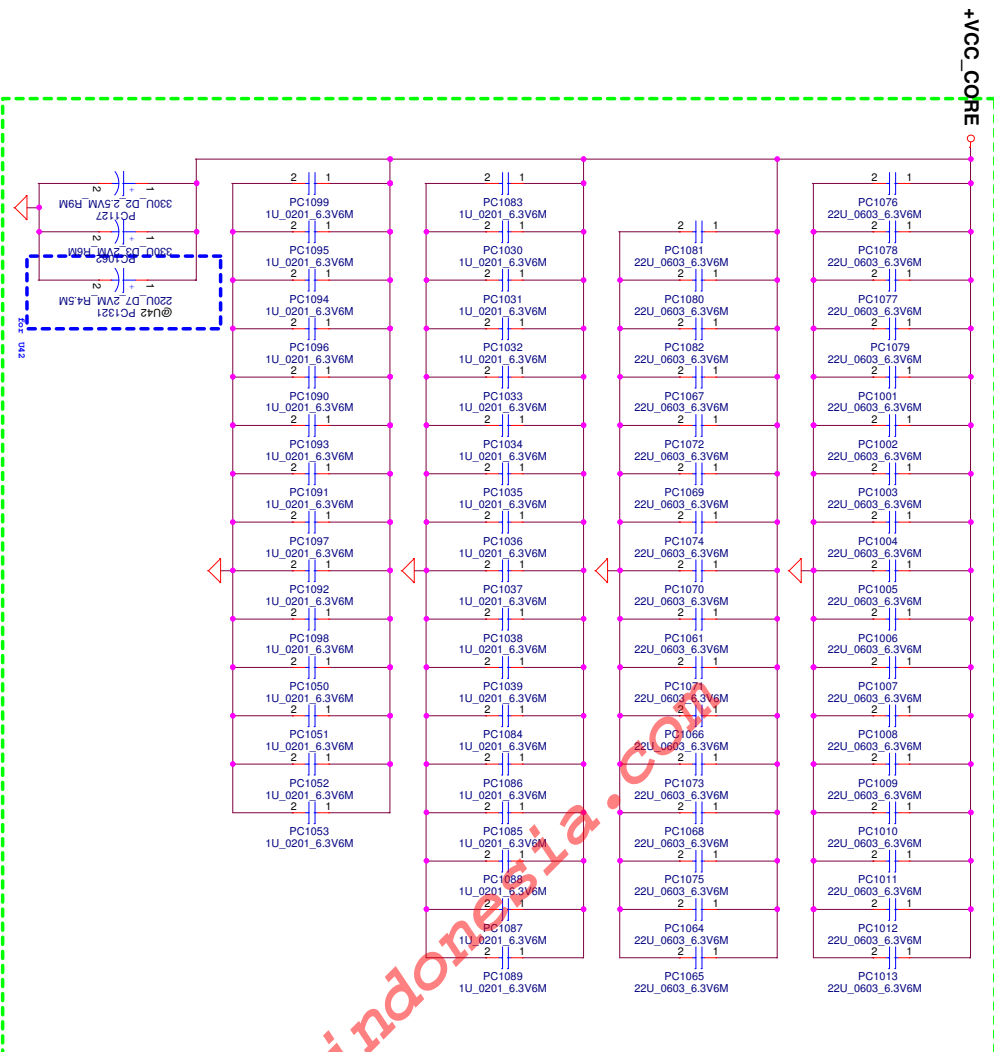


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File	PWR_VCORE_ISL95857		
Size	Document Number	LA-F311P	
Date	Wednesday, December 20, 2017	Sheet	48 of 58
Rev	2.0		

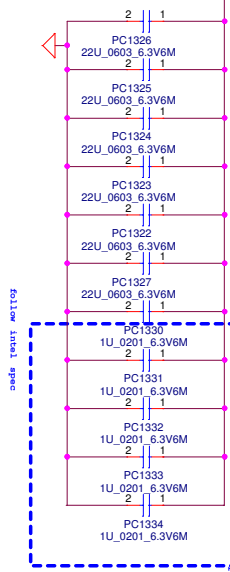
VCC_CORE Place on CPU (U22)
22U_0603 * 33 pcs +1U_0201*31 pcs
+330u_D2*2 pcs

VCC_CORE Place on CPU (U42)
22U_0603 * 33 pcs +1U_0201*31 pcs
+330u_D2*2 pcs +220u_D7*1 pcs

+VCC_CORE



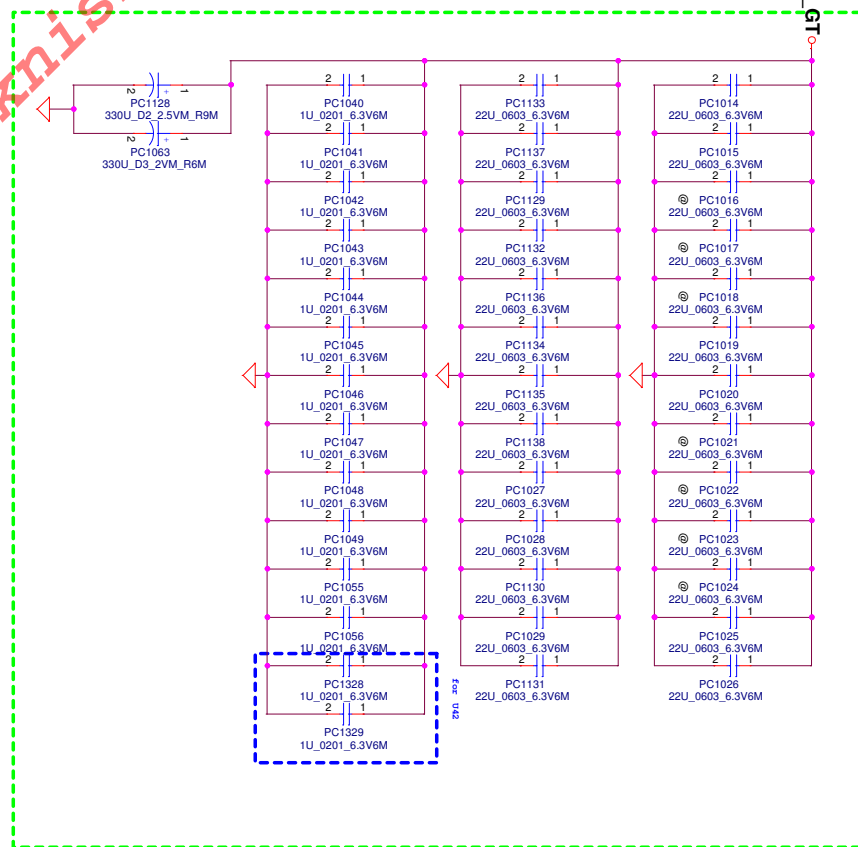
+VCC_GT +VCC_CORE



VCC_GT +VCC_CORE Place on CPU
22U_0603 * 6 pcs +1U_0201*5 pcs

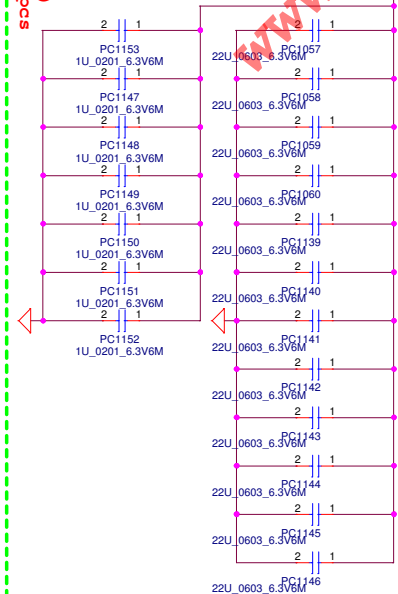
follow Intel spec

+VCC_GT



VCC_GT Place on CPU (U22)
22U_0603 * 19 pcs +1U_0201*14 pcs
+330u_D2*2 pcs

+VCC_SA



VCC_SA Place on CPU (U22/U42)
22U_0603*12 pcs + 1U_0201*7 pcs

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PROCESSOR DECOUPLING

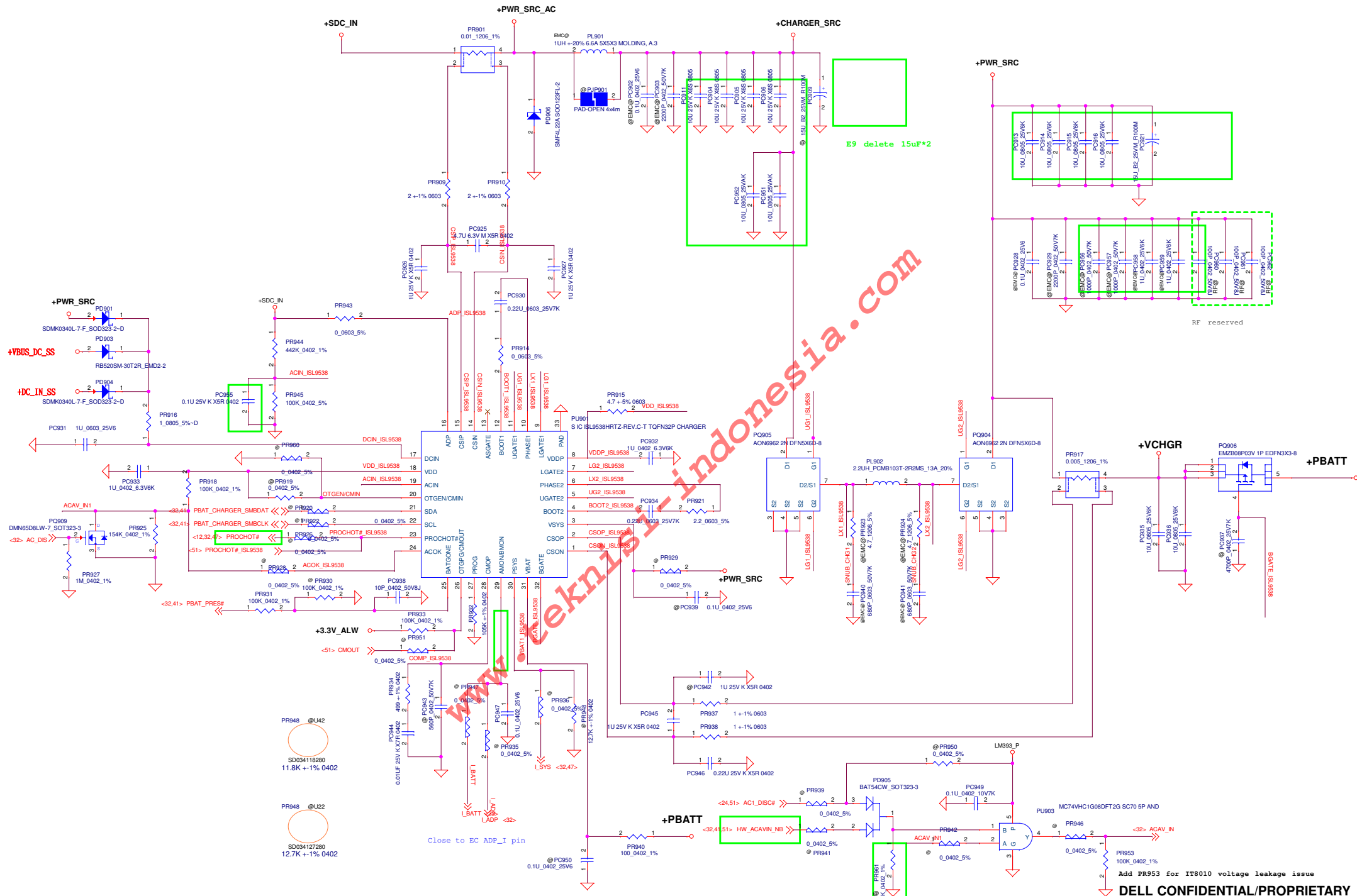
LA-F311P

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Add PR953 for IT8010 voltage leakage issue

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P59 PWR-Charger			
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	57	VCC_CORE VCORE_VGT,VSA	2017 06/07	Compal	Change DxmOS from TI to Fairchild	PU610/ PU612/ PU613 change to FDMF3035 (SA0000AHX00)	X01
2	50 51 52 53 56 57 59	+3.3V_ALW, +5V_ALW VCC_CORE VCORE_VGT,VSA Charger	2017 06/12	Larry	RF team request some item	Add PC315, PC314, PC960, PC961, PC962, PC700, PC701, PC142, PC143, Reserved PC316, PC12, PC702, PC141,PC695, PC696,PC224, PC703	X01
3	51 57 59	+3.3V_ALW, +5V_ALW VCC_CORE VCORE_VGT,VSA Charger	2017 06/12	Albert	EMI need to modify	1. Depop PC133, PC134, PC135, PC136, PC137, PC138, PC139, PC140, PC689, PC690, PC691, PC692, PC956, PC957, PC958, PC959. 2. Pop PL901.	X01
4	57 59	Charger	2017 06/12	Compal	Change component for acoustic solution	1. CPU input MLCC change to 0603 size and change to low noise MLCC (SE00000X210): PC608, PC612, PC656, PC657, PC658, PC664, PC665, PC672, PC673, PC674, PC675, PC682, PC683, PC684 2. Remove FC917-PC920(100*4pcs) , add FC921(15U pos cap)	X01
5	57	VCC_CORE VCORE_VGT	2017 06/19	Compal	Add one more bulk for acoustic solution	Pop 2pcs 100uf (PC606,PC607)	X01
7							
8							
12				Compal			
13				Compal			
14				Compal			
15				Compal			
16				Compal			
17				Compal			
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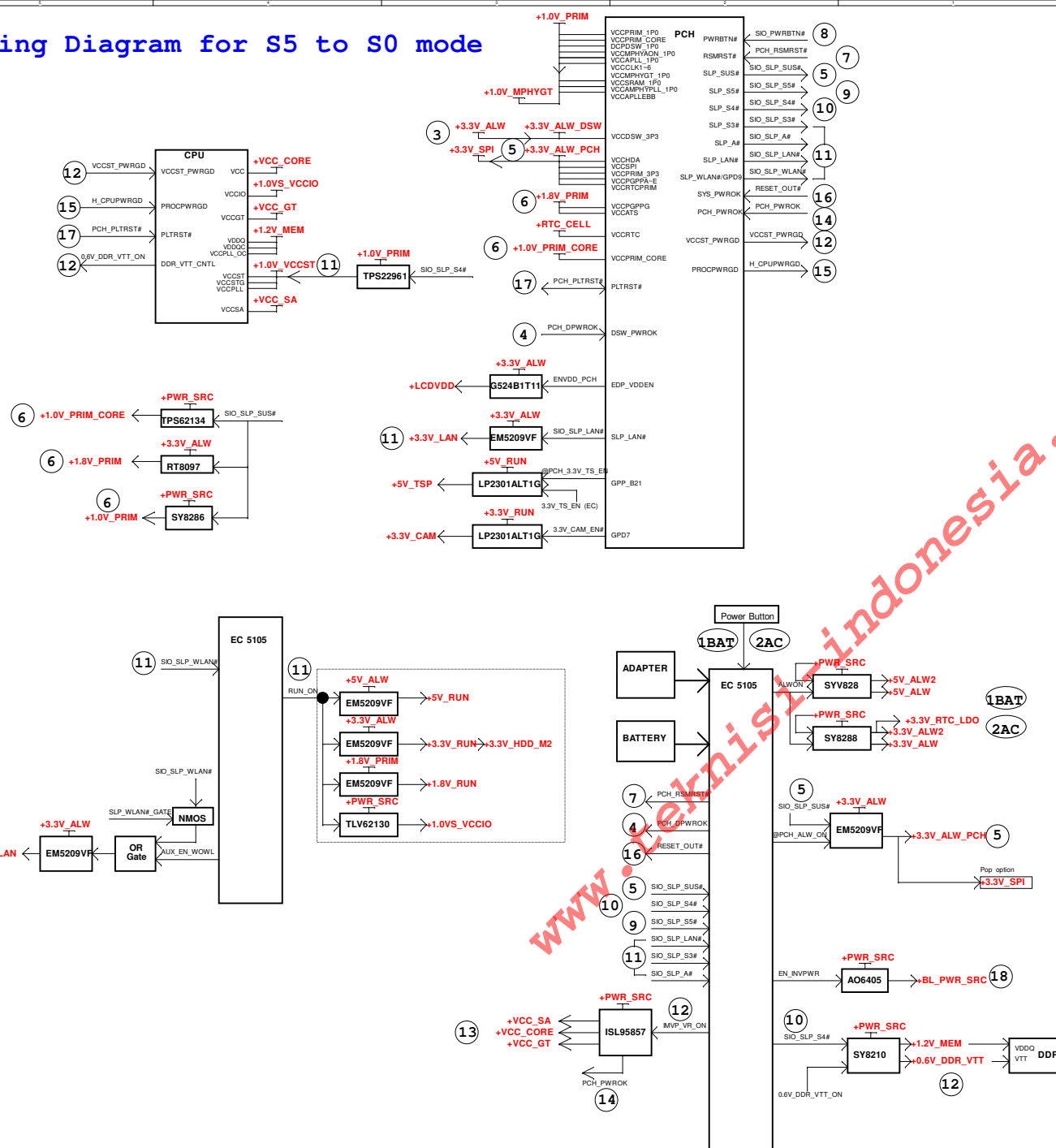
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PWR P.I.R

LA-F311P

25

Timing Diagram for S5 to S0 mode



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LA-F321P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	8	CPU (3/14)	2017/03/21	EE	Winbond 16MB SPI ROM EOL (change to J-die)	Change UC5, UC6 to SA00005VV20	0.1(X00)
2	8	CPU (3/14)	2017/03/21	ME	JSPI1 connector change vendor	Change JSPI1 to SP010022Q00	0.1(X00)
3	11	CPU (6/14)	2017/03/21	EE	KBL-R U42 X'tal	Add RC415~RC420,CC334,CC335,YC3	0.1(X00)
4	13	CPU (8/14)	2017/03/21	EE	KBL-R CRB schematic	Add RC436 0ohm to GND	0.1(X00)
5	14	CPU (9/14)	2017/03/21	ME	JXDP1 connector change vendor	Change JXDP1 to SP01001VB00	0.1(X00)
6	16	CPU (11/14)	2017/03/21	EE	Follow KBL-R_U42_Processor_Line_BGA1356_Ballout_Rev1p0	Reserve RC437, RC438	0.1(X00)
7	18	CPU (13/14)	2017/03/21	EE	RTC Power Gate Circuit for +3.3V_DSW	Add RC431~RC433, RC439, RC440, QC6, QC7	0.1(X00)
8	33	EC MEC5105	2017/03/21	EE	RTC Power Gate Circuit for RTCRST	Add QE14~QE17, RE540~RE546, RE551, CE63, RC441, RC442, DC1, DC2, RC445	0.1(X00)
9	34	EC MEC5105 Support	2017/03/21	EE	Remove IO expander	Remove UE2 relating circuit	0.1(X00)
10	28	eDP CONN & Touch screen	2017/03/21	ESD	ESD request	Remove DV7, DV8	0.1(X00)
11	35	USH & TPM	2017/03/21	EE	TPM NPCT65X and NPCT75X schematic colay	UZ12 relating circuit and change UZ12 to SA0000AQ200	0.1(X00)
12	31	NGFF Card	2017/03/21	RF	RF request to align w/ BR MLK	LI8, LI9 change to SM070003Z00, LI16, LI17 change to SM070003V00	0.1(X00)
13	33	EC MEC5105	2017/03/21	EE	RTCRST_ON glitch	Reserve CE64	0.1(X00)
14	A11	All	2017/03/21	EE	Port map change	JUSB1 change to USB30_port6 and USB20_port9 USB20_port1 BOM option to Type-C(PD UT5) Delete PS8338 and WIGIG circuit and connect DDI2 to UT1 (Pop RT29 and change net name to CPU_DP2_HPDP)	0.1(X00)
15	22	TBT-AR-SP (1/2) DP, FCIE	2017/03/21	EE	Reserve 0ohm for YT1	Add RT394	0.1(X00)
16	24	[Type C]PD Controller TI	2017/03/28	EE	Change PD to PD3.0	Change UT5 to SA0000AP500	0.1(X00)
17	9	CPU (4/14)	2017/03/28	EE	JUART1 reverse	JUART1 pin SWAP	0.1(X00)
18	33	EC MEC5105 Support	2017/03/28	EE	Panel ID define change	RE300 change to 130K ohm for 12" RE300 change to 62K ohm for 13"	0.1(X00)
19	34	USH & TPM	2017/03/28	EE	Prevent POA_WAKE# ESD	Add RZ364 100 ohm to POA_WAKE#	0.1(X00)
20	34	USH & TPM	2017/03/28	EE	Prevent Contactless_det# backdrive	Add DZ8	0.1(X00)
21	26	[Type C]USB3.0 CONN	2017/03/28	ESD	ESD request	Change DT7, DT8, DT11, DT12 to DT39 Change DT15, DT16, DT19, DT20 to DT40	0.1(X00)
22	11	CPU (6/14)	2017/03/28	EE	RTC Power Gate Circuit option	Add RC441, RC442, DC1, DC2, RC445	0.1(X00)

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23	A11	All	2017/03/28	EE	GPIO map change	PCH_RSMRST#_GPIO204 -> USH_PWR_STATE# (delete RE363) PORT80_DET# -> DCIN1_EN (delete RE512,RE513,RZ131) SHD_IO3 -> VBUS1_ECOK SHD_IO1 -> SATA_LED_EN ENVDD_PCH -> DCIN2_EN SIO_RCIN#_EC -> VBUS2_ECOK and delete RE339/RC13 USH_SMBCLK -> USH_EXPANDER_SMBCLK USH_SMBDAT -> USH_EXPANDER_SMBCLK Delete RTCRST_ON_GPIO141 PRIM_PWRGD_GPIO024 -> RESET_IN# 3.3V_TS_EN rename to PCH_3.3_TS_EN SHD_IO0 change to 3.3V_TS_EN and delete RE366 and PU 100K RE547 Add RV323/RV324 for 3.3V_TS_EN/PCH_3.3V_TS_EN option	0.1 (X00)
24	22	TBT-AR-SP (1/2) DP, PCIE	2017/03/30	EE	Intel review	RT39 change to 4.75K_0402_0.5%	0.1 (X00)
25	A11	All	2017/03/30	EE	GPIO map change	PANEL_ID -> SYSTEM_ID SHD_IO1 -> SATA_LED_EN -> MASK_SATA_LED# EXPANDER_GPU_SMDAT -> VCCDSW_EN_GPIO and delete RE524 EXPANDER_GPU_SMCLK -> free and delete RE525 THERMATRIP1# -> THERMTRIP1# THERMATRIP2# -> THERMTRIP2# SIO_EXT_SCI#_EC -> free and delete RE341 FAN1_TACH -> TACH_FAN1 LCD_TST -> free WWAN_RADIO_DIS# -> LCD_TST EC_GPIO123 (UE1.F12) -> WWAN_RADIO_DIS# DCIN3_EN -> EC_GPIO202 (UE1.J6) (SBMLK 12/13 only) FAN1_PWM -> PWM_FAN1 PS_ID -> free SHD_CLK -> PS_ID and delete RE374 AUD_NB_MUTE# -> NB_MUTE#	0.1 (X00)
26	A11	All	2017/03/30	EE	GPIO map change	UE1.B1 -> add net name 3.3V_ALW2 and depop RE57 (Microchip suggest) RESET_IN# -> Remove RE361 (Microchip suggest) SLOT2_CONFIG_3 -> NGFF_CONFIG_3 ME_FWP -> ME_FWP_PCH ME_FW_EC -> ME_FWP HW_GPS_DISABLE# -> GPS_DISABLE# VGA_ID -> BEEP H_PROCHOT# -> PROCHOT# USB_PWR_SHR_VBUS_EN -> USB_POWERSHARE_VBUS_EN USB_PWR_SHR_LFT_EN# -> USB_POWERSHARE_EN# SIO_EXT_SMI#_EC -> free and delete RE338 CLKRUN#_EC -> ENABLE_DS# and delete RE337 and add RE549, RE550 SHD_IO2 -> 1.8V_PRIM_PWRGD and delete RE360 BEEP -> VGA_IDENTIFY (rename from VGA_ID) SHD_CS# -> PCH_RSMRST# and delete RE364 SLOT2_CONFIG_0 -> NGFF_CONFIG_0 SLOT2_CONFIG_1 -> NGFF_CONFIG_1 SLOT2_CONFIG_2 -> NGFF_CONFIG_2 ACAV_IN_NB -> HW_ACAVIN_NB LID_CL#_NB -> LID_CL_SIO# SYS_PWROK->reserved 0ohm RE548 and add netname to RESET_OUT	0.1 (X00)

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27	All	All	2017/03/30	EE	Port map change	NGFF3 (SSD 4 Lane) add PCIE port 9 and port 10 LOM change to PCIE port 4	0.1(X00)
28	11 32	CPU (6/14) EC MEC5105	2017/04/05	EE	Intel PDG for DSx and NonDSx	Add RC443, RC444 for SUSACK#, ME_SUS_PWR_ACK Add BOM structure DS3@ for RE349 and RE536	0.1(X00)
29	17 40	CPU (12/14) Power control	2017/04/05	EE	PCH_PRIM_EN net name change	Change net name from SIO_SLP_SUS# to PCH_PRIM_EN	0.1(X00)
30	33	EC MEC5105 Support	2017/04/05	EE	Microchip suggest	Change RE71 to 10 ohm	0.1(X00)
31	40	Power control	2017/04/05	EE	+5V_RUN discharge circuit for S3 no power issue	Add QZ4 and RZ370	0.1(X00)
32	39	PAD, LED	2017/04/05	ME	Add bracket	Add bracket CLIP1 CLIP_14P0K2P6 Add bracket CLIP2 CLIP_7P7X4P2	0.1(X00)
33	33	EC MEC5105 Support	2017/04/11	EE	+5V_RUN for FAN	Change DE1 to SC400002J00	0.1(X00)
34	40	Power control	2017/04/14	EE	EC request to reseve OR gate for WLAN power EN	Reserve DZ9	0.1(X00)
35	33	EC MEC5105 Support	2017/04/14	EE	EC request to reseve ESPI_RESET# for JESPI	Reserve RE560	0.1(X00)
36	32	EC MEC5105	2017/04/14	EE	Schmatic align	Add GPU_SMCLK/GPU_SMDAT PU to RPE12	0.1(X00)
37	11	CPU (6/14)	2017/04/14	EE	WIGIG feature remove	Add back RC50 and depop	0.1(X00)
38	31	CodeC ALC3246	2017/04/14	EE	Realtek request	CA54 change back to 10pf and depop	0.1(X00)
39	32 11	EC MEC5105 CPU (6/14)	2017/04/14	EE	RTC power Gate circuit rev.2 (0411)	Delete RE540, RE542, RE544, RE545, QE14, QE16 Change RE543 to 1M ohm and RE546 to 10K ohm Add DE2, CE65, Reserve CE66 for VCCDSW_EN	0.1(X00)
40	11	CPU (6/14)	2017/04/14	EE	RTC Power Gate Circuit option (0411)	RC445 change to connect to VCCDSW_EN and pop	0.1(X00)
41	13	CPU (8/14)	2017/04/19	EE	KBL-R CRB schematic	Add BOM structure for RC436 U42@	0.1(X00)
42	All	All	2017/04/19	EE	GPIO map change	RC443 BOM structure change to @ GPIO126->GPU_PWR_LEVEL Add RTCRST_ON_R net neme for QE17.2 Add SIO_SLP_SUS#_R net name and PU RE561 SYS_LED_MASK#->LED_MASK# RC27.2->NC for CLKRUN# HDD_DET#->SATAGP0 Add RV326 and depop RC282/RE547 for 3.3V_TS_EN/PCH_3.3V_TS_EN	0.1(X00)
43	34	USH & TPM	2017/04/19	EE	TPM change to NPCT650x	Change UZ12 to SA00008EL80 and related resistors	0.1(X00)

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44	32	EC MEC5105	2017/04/19	EE	Dell request to add test point for EC free pins	Add test point T141 for UE1.D1->GPIO051 Add test point T142 for UE1.L11->GPIO054 Add test point T264 for UE1.F13->VBUS3_ECOK Add test point T143 for UE1.K7->GPIO011 Add test point T144 for UE1.M1->GPIO100 Add test point T262 for UE1.J6->DCIN3_EN Add test point T147 for UE1.M4->GPIO013	0.1 (X00)
45	A11	All	2017/04/20	EE	GPIO map change	GPIO013 net name change to DGPU_PWROK UPD1_ALERT#->UPD1_SMBINT# UPD1_SMBUS_ALERT#->UPD1_SMBINT#_R	0.1 (X00)
46	11	CPU (6/14)	2017/04/20	EE	Schematic align	INTRUDER# PU change to +RTC_CELL_PCH	0.1 (X00)
47	32	EC MEC5105	2017/04/26	EE	GPIO map change	UPD2_ALERT#->UPD2_SMBINT#	0.1 (X00)
48	11	CPU (6/14)	2017/05/03	EE	CLKREQ align	Pop RC50	0.1 (X00)
49	40	Power control	2017/06/02	EE	EC request to reseve OR gate for WLAN power EN	Add QZ15 and RZ518 Add SLP_WLAN#_GATE net and RE552 to UE1.K10	0.2 (X01)
50	24	[Type C]PD Controller TI	2017/06/02	EE	PD ROM main source change	UT6 change to SA000095R10 (GD)	0.2 (X01)
51	11	CPU (6/14)	2017/06/02	EE	Schematic align	Reserve RC551 for SUSACK#_R	0.2 (X01)
52	34	USH & TPM	2017/06/02	EE	Nuvoton request to change TPM_PIRQ# power rail TPM change to NPCT750	TPM_PIRQ# power rail change to +3.3V_ALW_PCH Change UZ12 to SA0000AQ200 and related resistors and CZ75 change to 10U	0.2 (X01)
53	A11	All	2017/06/02	ESD	Main source change	DI1,DI4,DT39,DT40 change to SC300001Y00 DI2,DI5 change to SCA00000T00 DA2 change to SCA00001A00 DT4 change to SCA00002Q00	0.2 (X01)
54	A11	All	2017/06/02	EE	DFX request	DA8, DC1, DC2, DE2, DZ1, DZ2, DZ5-DZ8 footprint change to AZ5125-01HPR7G_SOD523-2	0.2 (X01)
55	A11	All	2017/06/02	EE	Dell request to change cap to L-end P/N	L-end P/N for all cap	0.2 (X01)
56	31	CodeC ALC3246	2017/06/12	EE	DFX request	LA13 footprint change to TAI-T_HCB2012KF-121T50_2P	0.2 (X01)
57	34	USH & TPM	2017/06/12	RF	RF request	Add CZ76/CZ77 (12pf/68pf) for +3.3V_RUN of UZ12 Add CZ78 (100pf) for +PWR_SRC of JUSH1	0.2 (X01)
58	33	EC MEC5105 Support	2017/06/12	EE	Board ID	Change RE79 to 130Kohm (rev. X01)	0.2 (X01)
59	9	CPU (4/14)	2017/06/14	EE	GPIO map change	Add TypeC_CON_SEL1/TypeC_CON_SEL2 for UC1.W4/UC1.AB3 Reserve RC553-RC556 for connector selection	0.2 (X01)
60	40	Power control	2017/06/14	EE	EC request to reseve OR gate for WLAN power EN	Change QZ15 to SB00000T000	0.2 (X01)
61	39	PAD, LED	2017/06/14	EMI	Crystal shielding can (YT1)	Add CLIP3-CLIP5	0.2 (X01)
62	31	CodeC ALC3246	2017/06/15	RF	RF request	Reserve CA78 for +5V_RUN_AUDIO	0.2 (X01)
63	24	[Type C]PD Controller TI	2017/06/21	EE	PD change to rer.C	UT5 change to SA0000AX700	0.2 (X01)

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64	39	PAD, LED	2017/07/31	EMI	Crystal shielding can (YT1)	Add SHDCAN and remove CLIP13-CLIP15	0.3 (X02)
65	27 32 18	eDP CONN EC MEC5105 CPU (13/14)	2017/08/04	EE	Reserve soft start solution	Reserve RV400, CV635 for QV8 Reserve CZ200, RZ380 for QZ1 Reserve CC340 for QC7 Reserve RE565 for QE15	0.3 (X02)
66	31	CodeC ALC3246	2017/08/04	RF	RF request to pop CA54 for 2MHz/4MHz noise	Change CA54 to 82pf and pop	0.3 (X02)
67	33	EC MEC5105 Support	2017/08/07	EE	Board ID	Change RE79 to 62Kohm (rev. X02)	0.3 (X02)
68	9	CPU (4/14)	2017/08/09	EE	TPM_PIRQ# GPIO map change	Add RC560 and reserve RC561 to TPM_PIRQ#	0.3 (X02)
69	33	EC MEC5105 Support	2017/09/15	EE	Board ID	Change RE79 to 4.2Kohm (rev. A00)	1.0 (A00)
70	12	CPU (7/14)	2017/09/15	EE	ME SW depop	Depop RC222, SW1, RC221 change to 0 ohm short pad	1.0 (A00)
71	34	USH & TPM	2017/09/15	EE	TPM change to MP version	UZ12 change to SA0000AQ220	1.0 (A00)
72	9	CPU (4/14)	2017/09/15	EE	GPIO map change	Depop RC330, RC331	1.0 (A00)
73	8	CPU (3/14)	2017/09/15	EE	Add solder mask	Add UC6 -NPM	1.0 (A00)
74	A11	All	2017/09/15	EE	0 ohm change to short pad	0 ohm change to short pad	1.0 (A00)
75	A11	All	2017/09/15	EE	Only support DS3 (0 ohm change to short pad)	Only support DS3 (0 ohm change to short pad)	1.0 (A00)
76	21 30	HDMI CONN NGFF card	2017/09/18	EE	DFX request	Add LV3, LV6, LV9, LV12 RI27, RI28, RI29, RI30, RI47, RI48, RI49, RI50 -NPM	1.0 (A00)
77	25	[Type C]PD Power	2017/10/03	EE	X1 Code	DT1,DT2,DT3 Change from SC1N4148180 to SC100005500	1.0 (A00)
78	28	LAN Clarkvillie & RJ45	2017/10/03	EE	Not completely replaced with DAZ40	LL1 Change from SHI0000IY00 to SHI0000K000	1.0 (A00)
79	24	[Type C] PD Controller TI	2017/11/10	EE	Main vendor EOL	CT74,CT83 Change from SE000000U00 to SE00000QL10	1.0 (A00)
80	24	[Type C] PD Controller TI	2017/11/10	EE	PD just change part number	UT5 Change from SA0000AX700 to SA0000BIJ00	1.0 (A00)
81	39	PAD, LED	2017/12/08	EE	SW3 main source change	SW3 main source change from SN111005800 to SN100005800	1.0 (A00)
82	17	CPU (12/14)	2017/12/08	EE	WHEA BSOD Intel request	CC202 change to 22uf for 4+2 CPU, but keep 1uf for 2+2 CPU	1.0 (A00)
83	17	CPU (12/14)	2017/12/20	EE	WHEA BSOD	Add CC341 22uf 0603, Depop CC202 22uf 0402	2.0 (A01)
84	33	MEC5105 support	2017/12/29	EE	Board ID	Change RE79 to 2Kohm (rev. A01)	2.0 (A01)

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